Letters to the Editor

The Morphological Approach to Network and Circuit Design

G. S. MOSCHYTZ

I. Introduction

The purpose of this paper is to introduce the "morphological approach to discovery, invention and research" [1], [2] into the domain of network theory and circuit design. Some of the basic concepts of the morphological approach are introduced, using previously published results pertaining to the transistorized design of gyrators as an illustrative example. It is shown how all of the previously published transistorized gyrator designs, and many new ones in addition, can be obtained by this method. This is a typical characteristic of the morphological approach to any problem. In a companion paper [3], the morphological method is used to provide solutions to the problem of designing very low-frequency (i.e., below 10 Hz) networks that are realizable in hybrid integrated form, i.e., with *RC* components limited in value by the state-of-the-art hybrid integrated circuit technology.

II. The Morphological Box

The morphological approach to discovery, invention, and research was introduced by F. Zwicky [4], a highly successful scientist in the fields of astronomy, physics, and jet propulsion systems. Zwicky applied the morphological method to each of the above-mentioned fields thereby making valuable contributions to the theory and understanding of supernovae and inventing some of the earliest jet engines, including the jet-assisted takeoff (JATO) units used to launch heavyladen aircraft from short runaways. Later he applied the morphological approach towards the solution of all manner of technical and nontechnical problems, from the development of propulsive power plants and propellants to a systematic method of multilanguage teaching. In the following we shall demonstrate that this method can also be very well applied to the field of network and circuit design, using the design of transistorized gyrators as an illustrative example.

One useful tool in the morphological approach to problem solving is the *morphological box*. To use it we go through the following steps.

Step 1: Accurate formulation of the problem (e.g., design, construction, objectives) including all constraints.

Step 2: Characterization of the *m elements* (e.g., components, ingredients, parameters) $E_i (i = 1, 2 \cdots m)$, required for a solution of the problem. For any element E_i there may be n_i alternative elements such that we have n_i *element alternatives* E_{ij} with $j = 1, 2, \cdots n_i$.

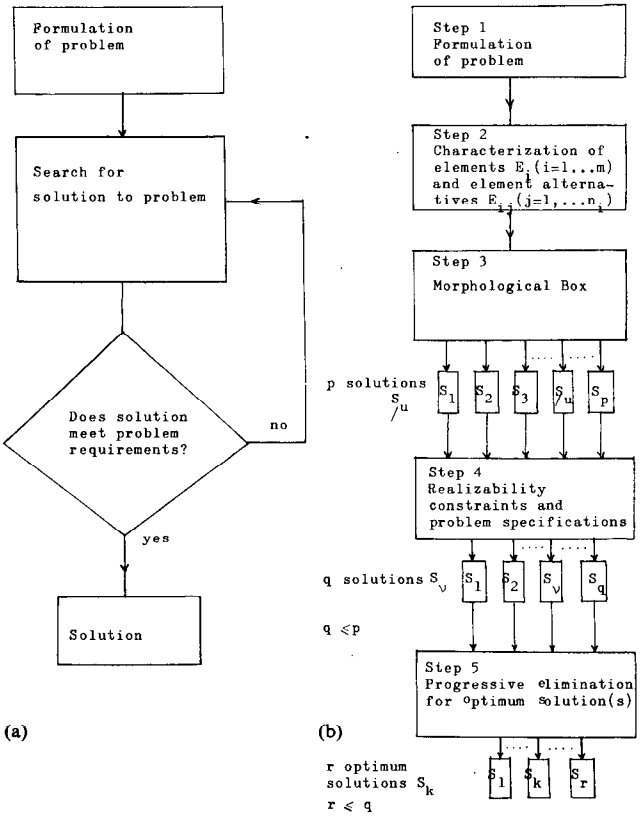


Fig. 1.

Step 3: Derivation of the multidimensional matrix, or *morphological box*, containing all of the solutions to the problem. Each solution corresponds to a different combination of element alternatives. The dimension of the matrix, or morphological box, corresponds to the number m of elements characterized in step 2.

Step 4: Evaluation of each of the solutions contained in the morphological box with respect to its realizability and to the objectives of the problem formulated in step 1.

Step 5: Selection and realization of those solutions that meet the realizability constraints and problem objectives. If only one solution is required all others are progressively eliminated until the "optimum solution" for the given problem has been found.

Note that whereas conventional problem solving involves finding *one solution* to a problem (see Fig. 1(a)), the morphological approach is to find *all possible solutions* at the same time and, depending on the realizability criteria and the requirements of

Manuscript received April 11, 1975; revised November 21, 1975.
The author is with the Swiss Federal Institute of Technology, CH-8006 Zurich, Switzerland.

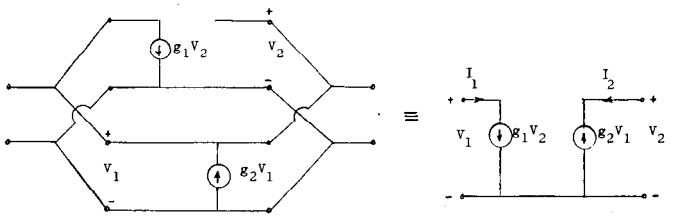


Fig. 2.

the problem, carrying out one or more of the acceptable solutions to their completion (see Fig. 1(b)). Conventional problem solving is a sequential process with a feedback loop while the morphological approach considers *all solutions* to a problem in parallel.

III. The Morphological Approach to Transistorized Gyrator Design

A gyrator can be interpreted as the parallel connection of two ideal voltage-controlled current sources (VCS) whose transconductances g_i $(i=1, 2)$ have opposite polarity (Fig. 2). The corresponding y matrix is

$$[y]=\begin{bmatrix} 0 & g_1 \\ -g_2 & 0 \end{bmatrix}. \tag{1}$$

To illustrate the morphological approach to the transistorized design of gyrators [5], [6] we carry out the five steps outlined above.

Step 1: The problem is to design a transistorized two-port whose y-matrix is given by (1). We may wish to add the additional constraint of minimizing the number of transistors.

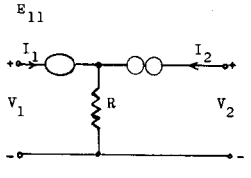
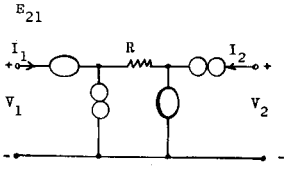
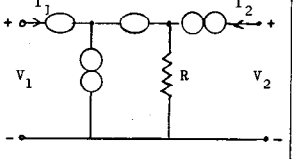
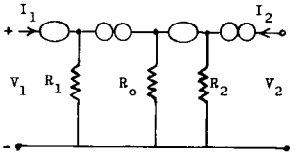
Step 2: We require two VCS's with opposite polarity. These are the two elements E_1 and E_2 required for the solution to our problem. The VCS's are to be transistorized, hence it is useful to start out with the equivalent nullor circuit [7] of a VCS, while taking care that each nullator-norator pair has a common terminal.

Note that more than one equivalent nullor circuit exists for a VCS. Assuming that a VCS with noninverting transconductance g_1, which we shall henceforth designate element E_1, can be represented by n_1 different nullor circuits, then we have n_1 element alternatives $E_{1j}(j=1,\cdots n_1)$ for our VCS E_1. Likewise with n_2 different nullor circuits for our VCS with inverting transconductance g_2 (element E_2), we have n_2 element alternatives $E_{2j}(j=1,\cdots n_2)$ for our VCS E_2. Incidentally, the derivation of these equivalent nullor circuits E_{1j} and E_{2j} is in itself a problem that can be approached morphologically.

In Table I we present two alternatives for each of our elements E_1 and E_2. Using the rules for nullator–norator manipulation [5] and proceeding morphologically, others can undoubtedly be found. The number of alternatives will be limited by the constraint imposed in step 1 of minimizing the number of transistors (i.e., nullors). If we limit ourselves to the minimum total number of nullors in E_1 and E_2 (which for a gyrator is three), the number of element alternatives is correspondingly small.

Step 3: Since we have only two elements E_1 and E_2, the morphological box will consist of a two-dimensional matrix (see Fig. 3). With n_1 and n_2 element alternatives, respectively, the number of solutions (i.e., transistorized gyrators) will be $p=n_1 \cdot n_2$. Each solution S_μ consists of a VCS $E_{1j}(j=1, 2\cdots n_1)$ connected in parallel with a VCS $E_{2j}(j=1, 2,\cdots n_2)$.

TABLE I
Equivalent Nullor Circuits for Voltage-Controlled Current Sources (VCS)

VCS with noninverting transconductance (Element E_1)	VCS with inverting transconductance (Element E_2)
E_{11}  $g_1=\frac{1}{R}$	E_{21}  $g_2=\frac{1}{R}$
E_{12}  $g_1=\frac{1}{R}$	E_{22}  $g_2=-\frac{R_o}{R_1R_2}$
E_{13} E_{1j} E_{1n_1}	E_{23} E_{2j} E_{2n_2}

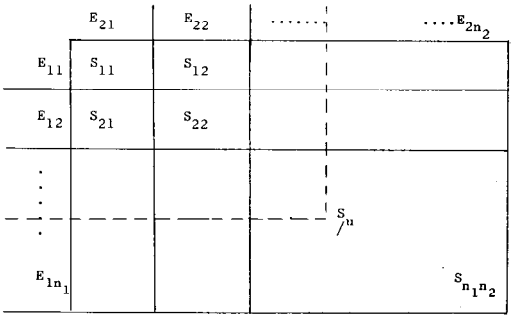


Fig. 3.

Step 4: We must now examine each solution S_μ of the morphological box and examine i) if it is physically realizable and ii) if, when realized in practice, it still provides the y-matrix of an ideal gyrator.

It is in this selection and realization process that the experience and ingenuity of the engineer (inventor) will count most. A solution that may be summarily dismissed as impractical if one adheres to conventional procedures and is biased by standard techniques may prove to be perfectly practical if one accepts the unconventional, and takes an unbiased approach to the problem.

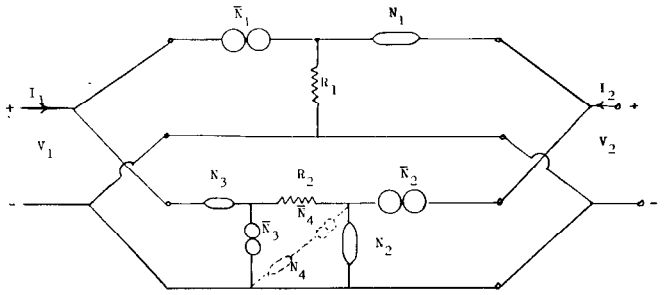


Fig. 4.

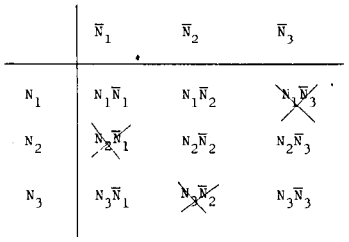


Fig. 5.

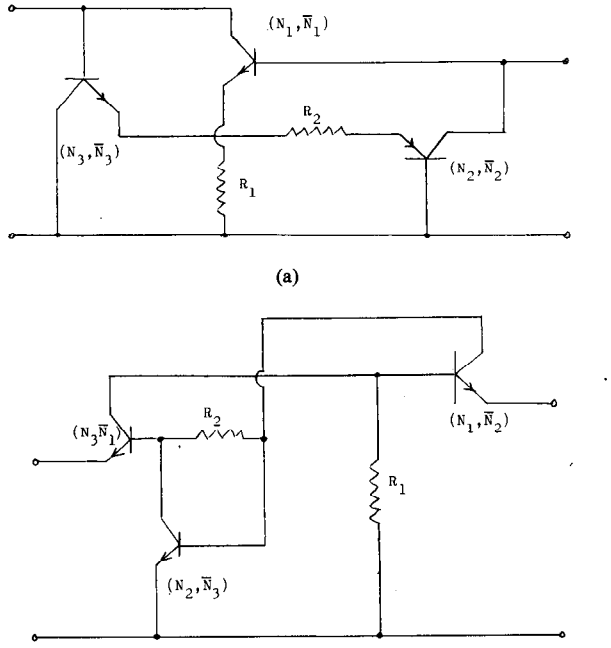


Fig. 6.

Let us, for example, consider the solution S_{11} of the morphological box. The equivalent nullor circuit of the resulting gyrator is shown in Fig. 4. The corresponding y-matrix is

$$[y]=\begin{bmatrix} 0 & 1/R_1 \\ -1/R_2 & 0 \end{bmatrix}. \tag{2}$$

In order to transistorize this circuit, nullator–norator pairs $(N_i, \bar{N}_j)$ must be combined such that they have a common node. This can again be approached morphologically. We require three transistors (elements) for each realization (solution). As we did in Table I, we must first characterize the elements at our disposal (step 2). This is best done in the matrix shown in Fig. 5. This matrix can be interpreted as a two-dimensional morphological box where we have two elements (namely, a nullator and a norator) and a realizable solution is a nullor with a common node. Those nullator–norator pairs that have no common node are not realizable as transistors and are crossed out in Fig. 5. Furthermore only those groups of three nullors can be used per gyrator that have neither a nullator nor a norator in common. Thus rather than derive the three-dimensional morphological box for the realization of our gyrator S_{11}, we can now pick those groups of three nullors in the matrix of Fig. 5 that have neither a row nor a column in common.

It is easy to see that there are only two solutions to this problem; the diagonal group $(N_1\bar{N}_1, N_2\bar{N}_2, N_3\bar{N}_3)$ which results in the transistor circuit of Fig. 6(a) and the group $(N_1\bar{N}_2, N_2\bar{N}_3, N_3\bar{N}_1)$ resulting in the transistor circuit of Fig. 6(b). More solutions can be obtained if we add nullator–norator pairs to the circuit of Fig. 4 such that it remains unchanged. This is the case for the additional nullor N_4, $\bar{N}_4$ shown in Fig. 4, since a nullator and norator in series corresponds to an open circuit [5]. Clearly such an additional nullor must be placed judiciously to provide as many useful transistor formations as possible. Furthermore each additional nullor violates our constraint of minimizing the number of transistors. With N_4 and $\bar{N}_4$ the matrix in Fig. 5 becomes a 4×4 matrix and each realizable solution, comprising four nullors having adjoining nodes, must be found.

We see from the above that each solution of our original morphological box (Fig. 3) may in turn provide a new group of solutions, each of which may be found morphologically. Many of the resulting solutions have been reported on individually [5], [6], [8], [9]; they were found in the conventional manner outlined in Fig. 1(a). With the morphological approach, *all* of the reported circuits can be found as well as many others. Having found them in the rudimentary form of Fig. 6, it remains to establish the proper biasing, p-n-p–n-p-n transistor combinations and other practical circuit details, necessary to obtain satisfactory performance when realized in discrete- or integrated-circuit form. As has been shown [10]–[12], this is by no means a trivial problem and again requires ingenuity and know-how on the part of the circuit designer. It is not our intention at this time, however, to pursue this discussion with a view to finding new transistorized gyrator circuits. We wish merely to introduce the morphological approach to problem solving into the field of network and circuit design, using the example of transistorized gyrator design as a vehicle to do so. In a separate paper [3], it is shown how this method can be used advantageously to design very low-frequency active filters suitable for hybrid integrated circuit implementation.

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A Simple Method to Determine the Characteristic Function $f(\lambda)=|\lambda I-A|$ by Discrete Fourier Series and Fast Fourier Transform

***Abstract*—A formula to determine the characteristic function of $N\times N$ matrix by discrete Fourier series is given.**

This letter presents a new algorithm in order to determine the widely used characteristic function of any $N\times N$ real or complex-valued matrix in various fields of engineering and applied mathematics. This algorithm also enables us to further investigate into some fundamental properties of the coefficients of the characteristic function.

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The author is with the Department of Electrical Engineering, Polytechnic Institute of New York, Brooklyn, NY.

A is a $N\times N$ matrix, the scalar polynomial

$$f(\lambda)=\det(\lambda I-A)=\lambda^N+\alpha_{N-1}\lambda^{N-1}+\cdots+\alpha_1\lambda+\alpha_0 \quad (1)$$

is the characteristic function corresponding to A.

Let $W=\exp(2\pi/N)j$ be the Nth root of unity. Then from (1), we obtain

$$f(W^{-m})=\det(W^{-m}I-A)=W^{-mN}+\alpha_{N-1}W^{-m(N-1)}+\cdots+\alpha_1W^{-m}+\alpha_0, \qquad m=0,1,2,\cdots,N-1 \quad (2)$$

since m and N are integers, therefore $W^{-mN}=(W^N)^{-m}=\exp(-2m\pi)j=1$ and from (2)

$$\det(W^{-m}I-A)-1=\alpha_{N-1}W^{-m(N-1)}+\cdots+\alpha_1W^{-m}+\alpha_0. \quad (3)$$

Let

$$b_m=\det(W^{-m}I-A)-1 \quad (4)$$

from (3) and (4), we have the form

$$b_m=\sum_{k=0}^{N-1}\alpha_kW^{-mk}, \qquad \text{for } m=0,1,2,\cdots,N-1.$$

Therefore

$$\alpha_k\overset{N}{\leftrightarrow}b_m$$

forms a discrete Fourier series pair. The inversion formula gives that

$$\alpha_k=\frac{1}{N}\sum_{m=0}^{N-1}b_mW^{-mk}, \qquad k=0,1,2,\cdots,N-1.$$

For large N and $N=pq$, α_k can be determined from p discrete Fourier series of order q (fast Fourier transform).

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