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TUNABLE CCII-MOSFET-C FILTER BIQUADS FOR VIDEO FREQUENCIES

Hanspeter Schmid George S. Moschytz

Signal and Information Processing Laboratory, Swiss Federal Institute of Technology, Sternwartstrasse 7, 8092 Zürich, Switzerland.
E-mail: schmid@isi.ee.ethz.ch

***Abstract* — This paper describes two related topics. First, it is shown how the concept of the MOSFET-C integrator can be extended to single-amplifier filter biquads. Then a new differential-input balanced-output current conveyor (CCII) is presented, which has two essentially symmetrical and balanced signal paths. Using this CCII, a 4th-order lowpass filter cascade suitable for on-chip tuning is presented, whose passband edge frequency is tunable from 2 MHz to 4.5 MHz and whose pole Qs are fine-tunable to within 5%. Our simulation shows that the filter's total harmonic distortion is below 1% and that the filter dissipates only 2 mW per pole pair at 3V supply voltage. Finally it is shown how bandpass and highpass filters can be built using the same technique.**

I. INTRODUCTION

Banu and Tsividis presented their continuous-time MOSFET-C integrator in 1983 [1]. They showed that building the integrator as a balanced circuit makes it possible to cancel the effects of the even-order nonlinearities of the MOSFET resistors used in the circuit, which considerably simplifies the integration of tunable filters. Several papers on this topic have been reprinted in [2].

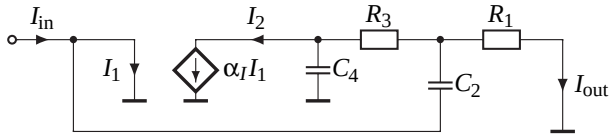

Figure 1: *Class 4* lowpass filter biquad (Sallen-Key filter) with a low-gain current amplifier ($\alpha_I < 0$)

In this paper, it is shown how the Banu-Tsividis technique can be applied to two classes of single-amplifier filter biquads discussed by Moschytz and Carlosena in [3]. Fig. 1 shows a current-mode Sallen-Key lowpass filter (designated *class 4* filter in [3]). We use the conventional definition of the current-controlled current source, as shown in Fig. 1 ($I_2 = \alpha_I I_1$). Note that this definition breaks the duality between voltage-mode and current-mode circuits, and the gain α_I must be *negative* for the feedback in a class 4-filter to have the proper sense.

The two resistors in Fig. 1 can be given identical values, $R_1 = R_3 = R$,[1] and the capacitors can be written as $C_2 = C/m$ and $C_4 = C \cdot m$, resulting in a current transfer function

$$T(s) = \frac{I_{out}}{I_{in}} = k\frac{\omega_p^2}{s^2 + \frac{\omega_p}{q_p}s + \omega_p^2}\,, \qquad \textbf{(1a)}$$

with

$$\omega_p = \frac{1}{RC} \qquad \textbf{(1b)}$$

$$\frac{1}{q_p} = 2m + \frac{1+\alpha_I}{m} \qquad \textbf{(1c)}$$

$$k = -\alpha_I\,. \qquad \textbf{(1d)}$$

It is apparent that the pole frequency ω_p and the pole quality factor q_p can be tuned independently by adjusting the resistors' value and the current amplifier's gain, respectively. This makes the filter suitable for on-chip tuning using two separate tuning circuits for ω_p and q_p.

In practice, the current amplifier in Fig. 1 has a relatively large input resistance $R_{in} = R/\kappa$ where, ideally, κ is ∞. With a finite κ, the transfer function of the filter becomes

$$T(s) = \frac{I_{out}}{I_{in}} = k\frac{\omega_p'^2}{\omega_z'^2}\frac{s^2 + \frac{\omega_z'}{q_z'}s + \omega_z'^2}{s^2 + \frac{\omega_p'}{q_p'}s + \omega_p'^2}\,, \qquad \textbf{(2a)}$$

with

$$\omega_p' = \omega_p\sqrt{\frac{\kappa}{\kappa+2}} \qquad \textbf{(2b)}$$

$$\frac{1}{q_p'} = \frac{1}{q_p}\sqrt{\frac{\kappa}{\kappa+2}} + \frac{1}{\sqrt{\kappa^2+2\kappa}} \qquad \textbf{(2c)}$$

$$\omega_z' = -\omega_p\alpha_I\kappa = -\omega_p'\alpha_I\sqrt{\kappa^2+2\kappa} \qquad \textbf{(2d)}$$

$$q_z' = -m^2\alpha_I\kappa\,. \qquad \textbf{(2e)}$$

Eqs. **(2a)**–**(2e)** show that a non-zero input resistance of the current amplifier has an influence on the pole location and also gives rise to a pair of complex zeros with high Q. This is not a problem as long as the zeros are sufficiently far away from the passband of the lowpass filter. Such zeros may even be advantageous, e.g. if they make the passband-stopband transition steeper.

Section II briefly discusses how the resistors in Fig. 1 can be replaced by MOSFET resistors such that the effects of their even-order nonlinearities cancel. In Section III, a new differential-input, balanced-output current conveyor (CCII)

[1] This is done here for the sake of simplicity. In practice, R_1/R_3 can be built as a ratio of sufficiently small integers by connecting "unity" MOSFET resistors in parallel.

structure is presented whose two signal paths have the same phase lag. A design example of a CCII and a 4th-order lowpass filter is presented in Section IV. Finally, SPICE simulations (using what we consider to be reliable transistor models) are given, and it is shown that the lowpass filter can readily be transformed into a bandpass and highpass filter.

II. MOSFET RESISTORS IN CURRENT-MODE BIQUADS

Tsividis presented several MOSFET resistor implementations in [4, Fig. 6]. Fig. 2 shows the MOSFET resistor circuit which is most suitable for current-mode circuits.

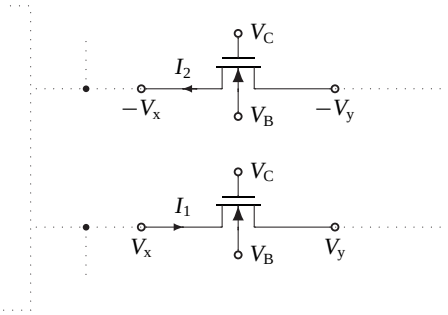

Figure 2: MOSFET resistor circuit. The dotted lines indicate the rest of the balanced filter circuit.

The bulks of both *n*MOS transistors are connected to the negative rail (in the filter example $V_B = -1.5$ V). The sheet resistance is controlled by the gate voltage V_C and has the value

$$R_\square = \frac{W}{L}\frac{2\left(V_x - V_y\right)}{I_1 + I_2} \approx \frac{1}{\mu C_{ox}(V_{CB} - V_T)} \quad \left[\Omega/\square\right], \quad \textbf{(3)}$$

where $V_{CB} = V_C - V_B$ and V_T is the transistors' threshold voltage at the operating point. If the voltages over the two transistors are balanced as indicated in Fig. 2, and the other filter components are perfectly matched, the balanced output signal is free of even-order harmonics. The odd-order harmonics of MOSFET resistors are much weaker and need to be compensated for only in low-distortion applications, for which a circuit with four MOSFETs has been shown in [1].

Tsividis pointed out in [4] that the voltage at the MOSFET resistor terminals should not exceed certain bounds. If any terminal voltage becomes higher than

$$V_{sw+} \approx V_C - \left(\phi_B - \frac{\gamma^2}{2} + \gamma\sqrt{(V_C - V_B) + \frac{\gamma^2}{4}}\right), \quad \textbf{(4)}$$

then the transistor enters the saturation region, and signal distortion rises rapidly. The increase in distortion is less abrupt for a voltage swing in the negative direction. If analog ground is at the midpoint between the rails, then it is safe to assume that the MOSFET resistor can be operated with a voltage swing of $\pm V_{sw+}$, which is about ± 250 mV for the process and the supply voltages used in the design example (*voltage swing condition*), provided V_C is close to the positive rail. This also imposes an upper bound on the resistances that can be obtained for a given maximum signal current, e.g. 5 kΩ for a maximum signal current of 50 μA.

These MOSFET resistors can readily be applied to the biquad filter shown in Fig. 1 by using a balanced current amplifier and connecting two identical versions of the MOSFET-C network to it. It can be shown, by analogy, that nonlinearity cancellation will also occur in this case. Banu and Tsividis pointed out that the main sources of nonlinearities in the circuits come from the practical device and balancing mismatches, and that the more accurately the signals are balanced, the better the performance of the circuits [5]. The results presented in [5] let us expect a resulting harmonic distortion of approx. 0.3% for a ±1% accuracy in output signal balancing, provided the voltage swing condition is met.

III. IMPLEMENTATION OF A FAST, BALANCED CURRENT CONVEYOR

Since our objective is to build a filter which is tuned on-chip, the amplifier does not have to be precise as such, but its two forward paths must be well balanced (i.e. at least to ±1%), and two identical amplifiers on the same chip should match as closely as possible.

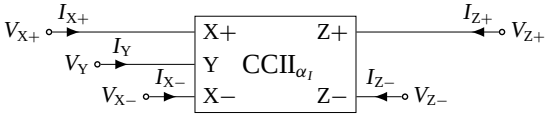

Figure 3: Symbol for the new balanced CCII

The amplifier needed to implement balanced current-mode *class 4* filters, i.e. a low-gain current amplifier with virtual ground at its input, is, in principle, a generalised *current conveyor of the second generation* (CCII), whose circuit symbol is shown in Fig. 3. It has one voltage input Y, two differential current inputs, $X+$ and $X-$, and two balanced current outputs, $Z+$ and $Z-$. In the ideal case, this CCII is described by

$$\begin{bmatrix} V_{X+} \\ V_{X-} \\ I_Y \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \alpha_I & -\alpha_I & 0 & 0 & 0 \\ -\alpha_I & \alpha_I & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} I_{X+} \\ I_{X-} \\ V_Y \\ V_{Z+} \\ V_{Z-} \end{bmatrix}. \quad \textbf{(5)}$$

The CCII is usually assumed to have a current gain of unity,[2] in our case we permit a general positive or negative current gain of α_I.

The class AB CCII shown in Fig. 4 is based on a structure proposed by Bruun [6]. It consists of an input voltage buffer with two outputs (M 1–M 6), several class AB current mirrors (M 7–M 20) and some additional circuitry to enhance

[2] A CCII with $\alpha_I = +1$ is usually called *CCII+*, a CCII with $\alpha_I = -1$ is called *CCII−*.

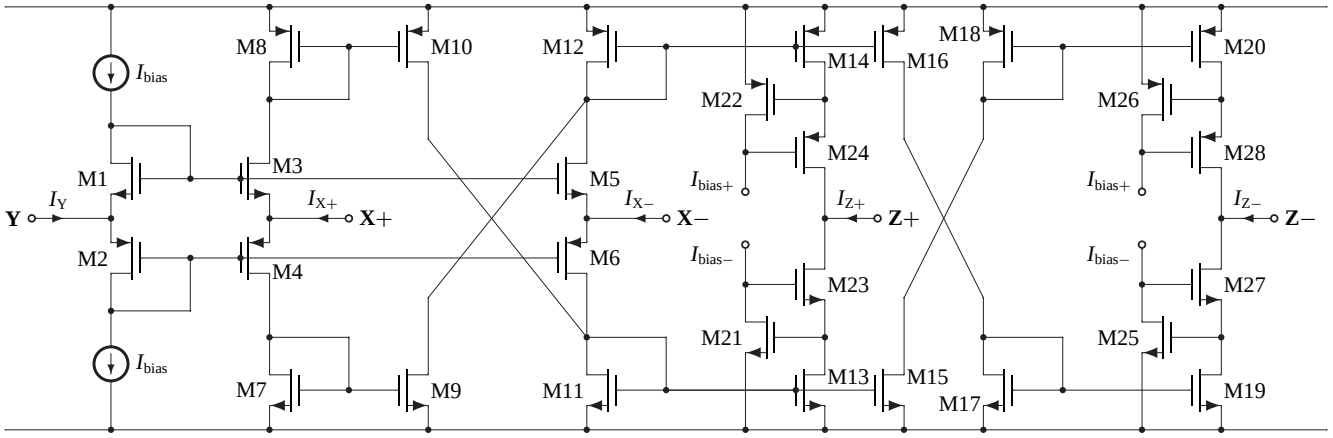

Figure 4: Balanced class AB current conveyor (CCII−)

the output resistance at $Z+$ and $Z-$ (M 21–M 28). Its operation principle is simple: the currents flowing into $X+$ and $X-$ are subtracted, the difference is then amplified and both sourced out of $Z+$ and sunk into $Z-$.

In more detail: if Y is connected to analog ground (typically the midpoint between the rails), then M 1–M 6 hold the current inputs $X+$ and $X-$ at virtual analog ground. Current flowing into $X+$ is copied by M 7, M 9 and flows through M 12. In contrast, current flowing *out* of $X-$ also flows through M 12; therefore the two signal currents are subtracted. The difference is then amplified by the double-output current mirrors M 11–M 16 and inverted again by M 17–M 20. Current flowing into $X+$ is therefore amplified, sourced *out of* $Z+$ and *sunk into* $Z-$. This makes the gain $\alpha_I < 0$, as required.

The gain of the stage M 11–M 16 can be tuned by changing the widths of (some of) the transistors M 11–M 16. *Since tuning the gain only changes* q_p, which does not have to be as precise as ω_p, it is sufficient to implement the variable-width transistors by connecting several transistors in parallel and switching the unused ones off.

An important feature of this CCII is the symmetry of its two forward paths, which is not immediately apparent. A closer look at Fig. 4 reveals that the same number and type of stages lie between $X+, Z+$ (input-inverter-adder-output) and $X-, Z-$ (input-adder-inverter-output). This means that both signal paths will have essentially the same phase lag, which is important for achieving non-linearity cancellation as discussed in Section II.

Improving input and output resistances

Small-signal analysis shows that the input resistance at $X+$ is $R_{X+} \approx 1/(g_{m3} + g_{m4})$. It can therefore be improved in two ways: either these transistors are made wider, or a higher supply current is used.

A high output resistance at $Z\pm$ is easily realisable using so-called *regulated cascodes* (RGCs) [7]. Thus, for example, transistor M 19, the output transistor of a current mirror, is normally in saturation, but would, by itself, have too low an output resistance. M 25 and M 27 form a negative feedback loop around M 19 and make the drain-source voltage of M 19, $V_{DS\,19}$, almost independent of V_{Z-}, which greatly enhances the output resistance. The output resistance of the transistor group M 19, M 25, M 27 becomes

$$R_{out} = \frac{1}{g_{ds\,19}} \cdot \frac{g_{m\,27} g_{m\,25}}{g_{ds\,27}(g_{ds\,25} + g_{ds\,i})}, \qquad \textbf{(6)}$$

where $g_{ds\,i}$ is the output resistance of the bias current source. The output capacitance becomes [7]

$$C_{out} = C_{gd\,27}\left(1 + \frac{2g_{ds\,25} + g_{ds\,19}}{g_{m\,25}} + \frac{g_{ds\,27}}{g_{m\,27}}\right) + \left(C_{gs\,27} + C_{gd\,25}\right)\frac{g_{ds\,27}}{g_{m\,27}}. \qquad \textbf{(7)}$$

It can be seen that $V_{DS\,19}$ is always above V_T, the threshold voltage, limiting the possible output voltage swing. A lower $V_{DS\,19}$ could be achieved by using other regulation techniques [8], but for our purposes the simple RGC has a sufficiently large voltage swing, since the main voltage swing limitations come from the MOSFET resistors.

IV. DESIGN EXAMPLE

In this section, the design of a CCII with a gain of $\alpha_I = -1.6$ is presented and simulation results are shown. Finally a filter built using this CCII and MOSFET resistors is simulated.

The filter example presented later in this section is a 4th-order Chebychev filter with a cutoff frequency of 4 MHz and 0.5 dB ripple. It therefore consists of two biquadratic sections with pole Qs 0.71 and 2.94, respectively, which are built using identical resistors for better matching. To keep the capacitor spread of the first section low, **(1c)** is solved for $q_p = 0.71$ and $m = 1$, which results in the gain $\alpha_I = -1.6$ mentioned above. The ideal filter's coefficients and element values according to Eqs. **(2b)** and **(2c)** are shown in Table 1.

Note that the resistance must be high enough to make ω_z' sufficiently high. If the 4th-order filter is to have a minimum

stopband attenuation of 45 dB, then $\omega_z' > 15\omega_z'$ and therefore, according to Eq. **(2d)**, $\kappa > 9$. The resistors must not be too large either, since this would increase harmonic distortion, as explained in Sec. II. For a maximum signal current of 50 µA, the maximum resistance is 5 kΩ, and therefore the input resistance of the current conveyor must be smaller than 600 Ω, which can readily be obtained.

	ω_p [MHz]	q_p	m	$R_{1,3}$ [kΩ]	C_2 [pF]	C_4 [pF]
Sec. 1	2.39	0.71	1.00	5.0	13.5	13.5
Sec. 2	4.12	2.94	0.64	5.0	12.2	5.0

Table 1: Filter sections of a 4th-order, 4 MHz Chebychev filter with 0.5 dB ripple.

Some of the important parameters of the CMOS process used in this paper are given in Table 2. The size of the small *n*MOS transistors has been chosen based on matching considerations. All *p*MOS transistors are three times wider than their *n*MOS counterparts, so that they have approximately the same gate-source voltage and transconductance at the operating point. All transistors have their bulks connected to the appropriate rails.

Parameter	*n*MOS	*p*MOS	unit
$KP = \mu_{ox} \cdot C_{ox}$	$200 \cdot 10^{-6}$	$50 \cdot 10^{-6}$	A/V^2
V_{T0}	0.62	−0.58	V
"Small" transistors:			
W/L	10/1	30/1	µm/µm
$\beta = W/L \cdot KP$	$2 \cdot 10^{-3}$	$1.5 \cdot 10^{-3}$	A/V^2

Table 2: Transistor Parameters of a 0.5 µm CMOS process

Design of a 50 µA CCII with gain $\alpha_I = -1.6$

The two most important design parameters of the CCII are the bias current and the size of the input transistors. The transistors M 1–M 6 are chosen to be large enough to ensure a low $X\pm$ input resistance and a high voltage swing, but small enough for sufficient speed. It follows from the well-known expressions for g_m that $R_{X+} < 600\,\Omega$ requires aspect ratios of approximately 100/1 and 300/1 for *n*MOS and *p*MOS, respectively, at an input bias current of 50 µA. All other transistors are "small" (see Table 2), with the exception of M 13–M 15, which are 20% narrower to reduce the gain to −1.6. Unfortunately, we cannot provide a closed formula for the expected speed of the CCII, since there is no *dominant* pole, only high-frequency parasitic poles and zeros. The time constant coming from the node between M 4 and M 7, $\tau \approx C_{total}/g_{m4}$, lets us expect a cluster of poles and zeros around 100 MHz.

The input stage's bias network is designed such that the drain current of M 3–M 6 becomes approximately 50 µA. In the RGCs, the transistors M 13, M 14, M 19 and M 20 must remain in saturation for maximum signal currents. According to [7], the RGCs' bias current must then be

$$I_{bias} \geq \frac{\beta'}{2}\left(|V_{GS\,max}| - 2\,|V_{T0}|\right)^2 , \qquad \textbf{(8)}$$

where $V_{GS\,max}$ is the gate-source voltage for the maximum drain current $I_{D\,max}$ and β' denotes the β of the transistors M 21, M 22, M 25 and M 26 for the RGCs built around M 13, M 14, M 19 and M 20, respectively. The difference in **(8)** means that if inequality **(9)** is satisfied, then the RGC could in principle (but not in practice) be driven with zero bias current.

$$|V_{GS\,max}| \approx \sqrt{\frac{2I_{D\,max}}{\beta}} + |V_{T0}| \quad < \quad 2\,|V_{T0}| \qquad \textbf{(9)}$$

Inequality **(9)** is indeed satified by all transistors even at $I_{D\,max} \approx 200\,\mu A$, and a reasonably small bias current, say 10 µA, is chosen for the RGCs. The voltage swing at the output becomes

$$V_{sw\,Z} \approx 1.5V - 2\sqrt{\frac{2I_{D\,max}}{\beta}} - |V_{T0}| \approx 400\,mV, \qquad \textbf{(10)}$$

meaning that the CCII can drive up to 4 kΩ with full signal current while maintaining a high output resistance. This was confirmed by a simulation.

Simulation results

Simulation results of the CCII with loaded outputs (1 kΩ in parallel with 10 pF) are shown in the Figs. 5–7. BSIM 3v3 transistor models of a real 0.5 µm CMOS process have been used for all simulations. The current transfer function and input impedance were obtained by applying a balanced step transient to the input (±50 µA) and calculating the Fourier transform of the derivative of the appropriate signals. (Note that the signal paths are balanced very accurately). The output impedance was obtained from an AC analysis at the operating point.

The CCII does not have a dominant pole. It can be seen from a numerical pole-zero analysis that a cluster of poles and zeros from 50 MHz upwards produces a phase lag of over 5 degrees above 1.2 MHz. The conveyor could be made faster by increasing the bias current of the input stage and, if necessary, the bias current of the regulated cascodes (speed–power tradeoff).

The calculated value of $R_{X+} \approx 1/(g_{m3} + g_{m4}) \approx 400\,\Omega$ corresponds well to the simulated value of 540 Ω. A difference of 10 Ω between the two paths occurs because the two outputs of the voltage buffer are loaded differently: $X+$ with an inverter and $X-$ with an adder. This difference is negligible compared to the resistance R (see Section I). The simulations also confirm the output resistance and capacitance predicted by the Eqs. **(6)** and **(7)**, respectively.

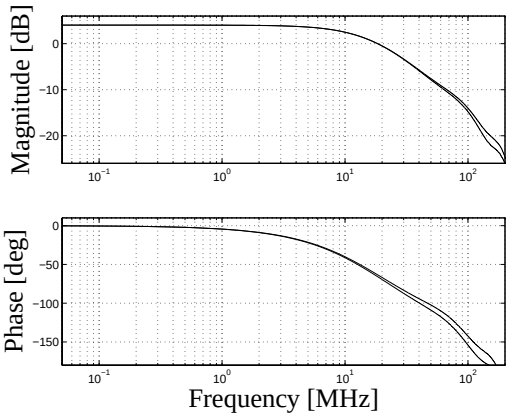

Figure 5: Current transfer functions from $X+$ to $Z+$ and from $X-$ to $Z-$

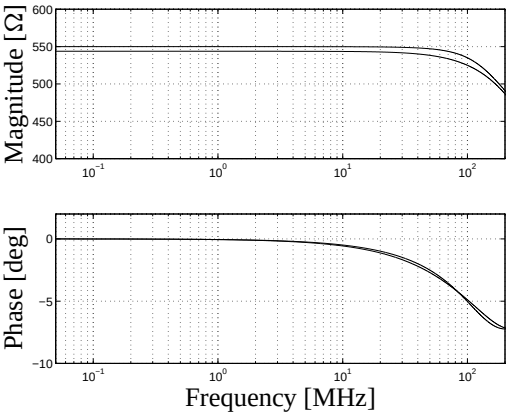

Figure 6: Input impedance at $X+$ and $X-$

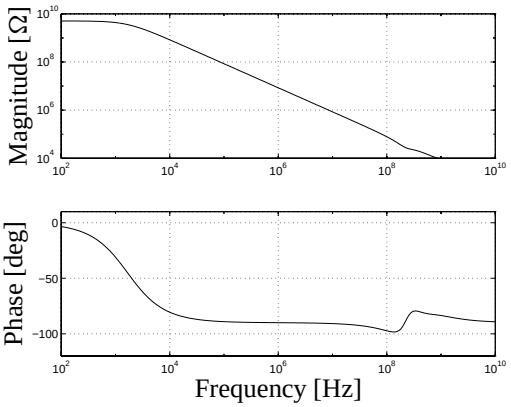

Figure 7: Output impedance at $Z+$ (without the RC-load)

Filter example: 4th-order equiripple lowpass filter

In this section, the filter example from Table 1 is designed and simulated. The sheet resistance of the MOSFET resistors can be calculated from **(3)**, where an approximate $V_T \approx 1.1$V is obtained by simulation. This can be used as a starting point for simulations which suggest using a transistor size of $W/L = 20\,\mu\text{m}/3\,\mu\text{m}$.

Figs. 8 and 9 show the effects of varying the resistors and the gains of the CCIIs, respectively, for the purpose of tuning. The same tuning signals are applied to both filter sections. It can be seen that ω_p and q_p can be tuned almost independently. (The magnitudes of the three curves in Fig. 9 have been scaled to the same DC gain to emphasise the q_p-tuning effect.)

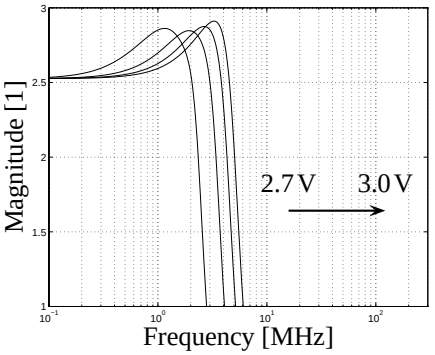

Figure 8: Transfer function for $V_{CB} = 2.7 \ldots 3.0\,\text{V}$

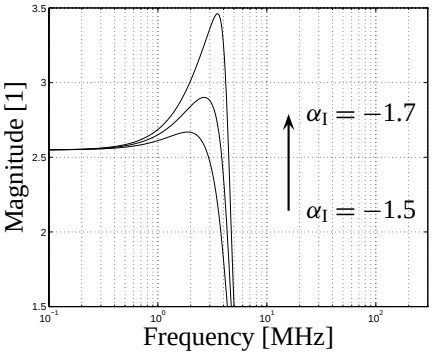

Figure 9: Transfer function for $\alpha_I = -1.5 \ldots -1.7$

The transfer function also has two pairs of complex zeros at 25 MHz and above, as expected. Increasing the frequency of the zeros further is not necessary here, since the attenuation is better than 45 dB over the whole stopband, which is sufficient for most practical applications in this frequency range.

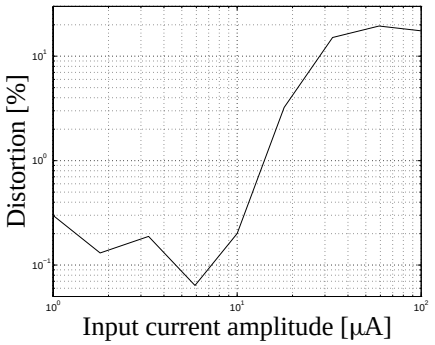

Figure 10: Total harmonic distortion versus input current for a 1 MHz signal.

As anticipated by the discussion in Section II, the main problem of this filter is harmonic distortion (THD), shown in Fig. 10 for a signal frequency at the upper edge of the filter's passband. For low signal magnitudes, the THD is

below 0.3 %, as predicted. Although this filter has not been specifically designed for low distortion, it can be used for various applications, e.g. video applications, since the THD does not exceed 1 % for input signal currents up to 14 μA (i.e. 35 μA at the output), a limit which is slightly lower than the theoretical value discussed in Sec. II.

Our simulation shows that this filter dissipates about 2 mW per pole pair. Furthermore, analytical results obtained by Bruun [9] suggest that the filter will have a signal-to-noise ratio of 60 dB.

These simulation results can be compared to measurements of a MOSFET-only bandpass filter recently published by Huang [10], which has a centre frequency of 560 kHz, a THD of 1 %, a dynamic range of 60 dB and a power consumption of 2.5 mW per pole pair at 5 V supply voltage. The filter presented in this paper has similar properties. It operates at higher frequency, from a lower supply voltage (3 V) and at lower power. However, our filter is also less precise if it is not tuned.

Lowpass, bandpass and highpass filters

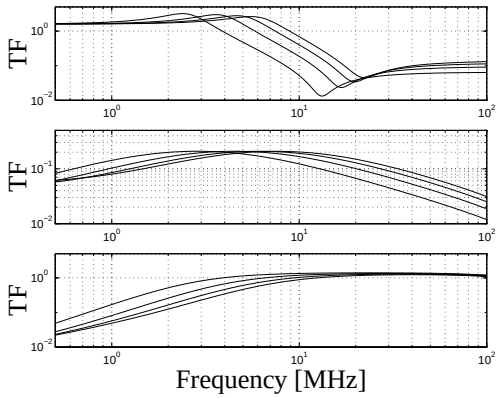

Figure 11: AC transfer functions (TFs) of a lowpass, a highpass and a bandpass filter biquad.

Finally, to show the feasibility of bandpass and highpass filters,[3] the passive components in Fig. 1 have been permuted as suggested in [3]: $R_3 \leftrightarrow C_4$ and $R_1 \leftrightarrow C_2$ for the highpass filter; $R_1 \leftrightarrow C_2$ for the bandpass filter, where R_1 has been doubled, C_2 connected to analog ground and and another identical resistor R_1' has been used to connect the node between R_3, C_2 and R_1 to the output. Fig. 11 shows the three transfer functions of the biquad section with $q_p \approx 3$.

It can be seen that by simply permuting the passive components, bandpass and highpass filter tunable over the same frequency range can readily be obtained. Because of the larger-than-zero input resistance of the CCIIs, the resulting reduced pole-Q values must be accounted for in the design process.

[3]The filter *class 4* in [3] actually comprises bandstop and notch filters as well, which can also be built as balanced MOSFET-C filters, but this is beyond the scope of this paper.

V. CONCLUSIONS

It has been shown in this paper how single-amplifier RC filter biquads can be converted to balanced MOSFET-C filters such that their pole frequency and pole Q are tunable independently. A new balanced current conveyor (CCII) has been presented which is suitable for implementing these filters in a 3 V CMOS process. Tuning takes place for the pole frequency by varying one control voltage and for the pole Q by switching the gain of some current mirrors in the CCII. A 4th-order lowpass filter example has been simulated, with a passband edge frequency tunable from 2 MHz to 4.5 MHz to an accuracy determined by the on-chip tuning circuitry, and pole Qs fine-tunable to within 5 %. The harmonic distortion and the noise of this filter are low enough e.g. for video applications, and the filter consumes only 2 mW per pole pair. Finally it has been shown that bandpass and highpass filters can also be built in the same way, using the same CCII.

ACKNOWLEDGEMENTS

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