Diss. ETH No 13878

Single-Amplifier Biquadratic MOSFET–C Filters

A dissertation submitted to the
Swiss Federal Institute of Technology, Zürich
for the degree of
Doctor of Technical Sciences

presented by

Hanspeter Schmid

dipl. El.-Ing. ETH
born on February 8, 1969
citizen of Härkingen SO

accepted on the recommendation of
Prof. Dr. George S. Moschytz, examiner
Prof. Dr. Qiuting Huang, co-examiner

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Für Alexandra

Denn die Summe unseres Lebens
sind die Stunden, wo wir lieben

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I wish to express my sincere gratitude to Prof. George S. Moschytz. He found the right balance between guiding me and giving me the freedom to pursue my own ideas, and thus made my doctoral studies a very productive and interesting time. I also thank Prof. Qiuting Huang for the constructive discussions about my work and for serving as the co-examiner of this dissertation.

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Our laboratory always felt like a second home for me, and I would like to thank *all* its members for that. I have had three very nice office colleagues during my doctoral studies; first Jossy Sayir, who who gave me so much when he suggested that I could play the trombone; then Drahoslav Lím and Felix Lustenberger, who both became good friends of mine. I would also like to thank Jürg Stettbacher, Marcel Joho, Max Dünki, and Martin Hänggi for the many interesting discussions about Life, the Universe, and Everything, and for all the fun we had together.

Last but not least, I would like to thank my parents, who paved my way, my wife Alexandra, who went along it with me and helped me through many difficult times, and to my son Matthias, who joined us in the middle and made everything so much nicer.

Abstract

This dissertation discusses the theory of single-amplifier biquadratic filters (SABs) and their implementation as CMOS video-frequency filters. It shows that building filters as cascades of single-amplifier biquadratic MOSFET–C sections is a viable alternative to using biquadratic Gm–C filter sections. The advantage of MOSFET–C SABs is that they typically use less chip area than a Gm–C filter with equivalent speed, distortion, noise, and power consumption.

The first part of this dissertation discusses the theory of integrated amplifiers, provides a new perspective of the current-mode vs. voltage-mode debate, and discusses the theory of SABs and the effects that amplifier non-idealities have on them.

The second part discusses second-order MOSFET–C networks and how to design filters with them, presents perfectly symmetrical video-frequency current amplifiers, one with fixed gain and one with variable gain, and contains measurement results of test circuits from two chips.

The third part presents a brief comparison of the MOSFET–C SABs presented in this dissertation to other video-frequency filters, and finishes with a discussion of design trade-offs and ideas for future research on the topic.

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Kurzfassung

Diese Doktorarbeit beschreibt die Theorie der biquadratischen Filter mit einem Verstärker (Single-amplifier Biquads, SABs) und ihre Implementation als CMOS Videofrequenzfilter. Sie zeigt auf, dass MOSFET–C SABs als Baublöcke für Filter höherer Ordnung eine gute Alternative zu den gängigen Gm–C Filterblöcken sein können, weil sie typischerweise eine kleinere Chipfläche benötigen, wenn sie auf dieselben Werte von Geschwindigkeit, Verzerrungen, Rauschen und Leistungsverbrauch ausgelegt sind.

Der erste Teil dieser Arbeit erläutert die Theorie der integrierten Verstärker, wirft neues Licht auf die Current-Mode–Voltage-Mode Debatte und diskutiert die Theorie der SABs und die Effekte, welche Nichtidealitäten der Verstärker auf diese SABs haben.

Im zweiten Teil werden MOSFET–C Netzwerke zweiter Ordnung besprochen, und es wird gezeigt, wie man damit Filter entwirft. Dazu werden perfekt symmetrische Videofrequenzverstärker eingeführt, einer mit festgesetzter und einer mit variabler Verstärkung. Der zweite Teil enthält auch diverse Messungen der Schaltungen von zwei Testchips.

Der dritte Teil enthält einen kurzen Vergleich der hier vorgestellten MOSFET–C SABs mit anderen Videofrequenzfiltern. Er beschreibt zusammenfassend die gegenseitigen Abhängigkeiten der beim Entwurf getroffenen Entscheidungen und der Leistungsmerkmale der Filter. Als Abschluss werden einige Ideen für zukünftige Forschungswege besprochen.

Contents

Chapter I

Introduction

Anything goes!

(Paul K. Feyerabend)

This dissertation consists of three parts. Part I, "The System Level," treats the theory of broad-band amplifiers and of single-amplifier biquadratic filters. Part II, "The Transistor Level," explains how MOSFET–C single-amplifier biquadratic filters work, how they can be designed, and which performance they can achieve. Part III, "Conclusions," contains a comparison of the MOSFET–C SABs to other filters (mainly Gm–C filters) and a discussion of open questions and options for future research.

The form of the text itself also has three main elements: the technical contents, marginal notes that can be understood as abstracts of single paragraphs, and a non-technical "Background" section in which the personal motivation and the history of every chapter is explained.

This first chapter gives a brief overview over analogue integrated filters and an outline of this dissertation.

1.1   Background

The main reason why I applied for a position as a doctoral student with Prof. George S. Moschytz was my interest in his lecture series "Analogue Signal Processing and Filtering (ASF)," which I visited in the last term of my electrical-engineering studies.

When I started my research project, Moschytz gave me the task to find out what the performance difference between current-mode and voltage-mode filters was. I found out very soon that, in theory, there was none. I spent several months with finding out how current-mode filters were built, and attempted to do a complete classification of single-current-conveyor biquads, only to find out that it did not answer the performance question.

So eventually I ended up designing current-mode SABs myself, because they were the best way (in my view) to build low-power video-frequency SABs in CMOS. Along the way, I also found arguments showing that there can be no general performance difference between current-mode and voltage-mode circuits, which answered the question I was asked at the start.

When Moschytz retired in the End of 1999, he asked me whether I could read his lecture series in Spring 2000. I very happily accepted this offer, not only because I like lecturing, but also because it appealed to the romantic part of me that my time at the Signal and Information Processing Laboratory of the ETH Zürich ended as it began, with "Analogue Signal Processing and Filtering."

When I started to prepare my lectures, I saw with surprise that my dissertation bases so heavily on that lecture that one could say, without being too unprecise, that the dissertation is an extension of ASF into the realm of integrated circuits.

Analogue integrated filters 1.2

There is a wide variety of analogue integrated filters in the literature, but there are only two operating principles behind the majority of these filters. Complex poles are either achieved by implementing RLC filters without using actual inductors, or by building an analogue computer that is capable of forming differences of rational expressions with real poles.

RLC simulation and differences of polynomials

One approach to form such differences is to build loops containing integrators; such filters are known as integrator-connected filters, state-space filters, and under other names. They are often implemented as Gm–C filters or as log-domain filters, although different integrators are sometimes used when special filter properties are needed. From a mathematical point of view, such filters can produce complex poles because two or more interlinked loops give the transfer function a denominator with three or more difference terms of polynomials having real zeros.

Integrator filters

Integrator-connected filters always require at least two amplifiers to generate one complex pole pair. In contrast, single-amplifier biquadratic filters form a difference of two second-order rational expressions with real poles. This is achieved by putting a second-order RC network in the feedback path of an amplifier.

Single-amplifier biquadratic filters

There are also two different ways of implementing RLC filters. One is to simulate every inductor using a gyrator circuit. Although gyrators are often built using opamps, they can also be built with OTAs, in which case the resulting filter again is a Gm–C filter. Such gyrator filters are mainly used because of their good sensitivity properties and good noise behaviour.

Gyrator filters

The other way of simulating RLC filters is the so-called FDNR (frequency-dependent negative resistor) synthesis, where the impedances of all elements in the RLC prototype are scaled by the factor ω_0/s, where s is the complex frequency of the Laplace domain. This transformation maintains the transfer function of the filter, but not its terminal impedances: all resistors are transformed into capacitors, the inductors into resistors, and the capacitors into so-called FDNRs. Since many gyrator implementations can also be used as FDNRs, there

FDNR filters

is not much difference between FDNR and gyrator filters. In fact, if it is not a problem whether the port impedances are transformed or not, the decisive question is whether the RLC prototype has more inductors or capacitors. In the latter case, the gyrator filter should be used, in the former case it is the FDNR filter.

SABs are
power-efficient
and small

However, RLC simulations also require at least two amplifiers per pole pair, so the single-amplifier biquads (SABs) that were already a good way to build cheaper discrete-component filters are also promising candidates for power-efficient, small integrated filters.

1.3   Outline of this dissertation

Theory of amplifiers
and filters

This thesis has three parts. Part I is mainly theoretical and gives an introduction into broad-band amplifiers, active-RC SABs, and the effects of amplifier non-idealities on SABs. The main contribution of Chapter 2 is the first amplifier classification that encompasses all operational amplifiers and current conveyors in a way that connects the most abstract theory to actual transistor circuits. It is also shown how all the discussed amplifiers can, in principle, be implemented with only a few basic CMOS cells. Chapter 3 shows the connection between current-mode and voltage-mode circuits by looking at the impedances of individual circuit nodes rather than at larger circuit blocks. The main results of this view are a new, constructive proof of the circuit transposition theorem and a discussion of "current-mode vs. voltage-mode" showing that there is no general performance difference between the two. Finally, Chapter 4 provides the first closed-form solution of the problem to minimise the variance of the pole Q of a Sallen-and-Key filter, and presents a comprehensive discussion of the effects amplifier non-idealities have on the transfer function of a Sallen-and-Key filter.

Implementation of
current amplifiers and
MOSFET–C networks

Part II is more descriptive, since the circuits shown there have been developed by combining several ideas that were already known in the literature. Chapter 5 discusses the function of second-order MOSFET–C networks and shows how to choose the analogue ground in order to optimise the harmonic

distortion of a MOSFET–C SAB. Furthermore, a charge-pumped MOSFET–C network is discussed, and a closed-form expression for the signal swing that optimises the signal-to-noise ratio for a given level of distortion is derived. The fixed-gain and variable-gain current amplifiers in Chapter 6 base on ideas introduced in Chapter 2; they differ from other implementations found in the literature in that they have two perfectly symmetrical balanced signal paths. Finally, Chapter 7 provides a description of several integrated test circuits and discusses measurements which show that MOSFET–C SABs really work.

Part III is the shortest part. It shows that our filters perform as well as other video-frequency filters but are smaller, and contains a brief discussion of design trade-offs in Chapter 8, and finally gives a discussion of open questions and ideas for future research in Chapter 9.

Trade-offs and open questions

Part I

The System Level

Chapter 2

Approximation of the universal active element

I shall pass from thousands of apparitions
to one alone: from a very complex dream
to a simple dream. Others will dream that
I'm mad, and I will dream of the Zahir.

(Jorge Luis Borges)

The main idea of this chapter is to bridge the gap between amplifier theory and amplifier design that has opened up in the past few years with the advent of a wide range of new, theoretical amplifier concepts. The gap is bridged with a hierarchical classification that has actual transistor circuits at its bottom and the most general of active two-ports, the universal active element, at its top. It is shown that the nullor and the CCII− described as four-terminal networks are two different universal active devices. A new definition of the term "operational" is given, nine different operational amplifiers are derived from the nullor, and twelve different current conveyors are derived from the CCII−. Finally, it is shown how all these amplifiers can be implemented in CMOS.

This chapter presents a new theoretical viewpoint that covers a wider range of amplifiers than previous classifications. As a side benefit, a new amplifier appears, the current-feedback OTA, which can be built from most current opamps without adding a single transistor.

2.1   Background

The line of thought that lead me to the amplifier classifi-
cation described below started at the ECCTD 97 in Bu-
dapest, the first conference I attended as a speaker. There
I listened to a talk about a filter synthesis method us-
ing a new theoretical amplifier concept. As it happens
sometimes in such papers, several building blocks con-
sisting of one such amplifier plus one resistor simply re-
alised a transconductor. So someone in the audience asked
the speaker why these blocks should be realised in the
speaker's way and not as OTAs. The speaker did not
even understand the question (why this was so will be-
come clear below). Much later in the same session, when
I had just finished my talk, something very unconventional
happened. Somebody from the audience asked me to clar-
ify the concepts used by the other speaker, and to say
whether the new amplifier was really new! I stalled as
well as I could under the circumstances.

At home, I read many more papers about new amplifiers,
and when I started to see how similar all these concepts
were, I became angry. I developed the feeling that there
was no real contribution in this papers, a feeling that
can clearly be seen between the lines of the internal re-
port I wrote soon afterwards [Schmid98a]. Also, my own
thoughts were not clear enough back then, neither was the
way I expressed them.

In the following two years, I wrote [Schmid98b] with the
help of Markus Helfenstein who pointed out to me which
parts displayed my feelings rather than my knowledge,
and then I wrote and re-wrote the publication several
times, discussing several versions of it with George S.
Moschytz, who helped me to bring it into the style (both
writing style and technical style) required for publications
in the IEEE Transactions on Circuits and Systems.

All these discussions also made me why the misunder-
standings at the ECCTD'97 had happened. The aim of
the theorist (the speaker) was to propose a new theoretical
amplifier concept that makes it possible to develop new
circuit synthesis methods. The question from the audi-

ence, however, was about the best possible practical implementation of a circuit synthesised with the new method, but it was asked in a way which made the speaker assume that the person asking him wanted to replace his theoretical amplifier by a theoretical transconductance element, which would have achieved nothing but taking down the basis on which the new synthesis method stood. Having seen this, my anger disappeared and gave way to a feeling of shame and then to the wish to provide both sides with a tool that would enable them to understand each other better. The result is this section, which also appeared in [Schmidoob] in a modified form.

Introduction   2.2

Circuit simulators such as Spice or Spectre process net-lists in which a circuit is described by elements such as resistors, capacitors, controlled sources, transistors, and so on. There is much redundancy in the set of elements provided by circuit simulators, since many of them can also be expressed as sub-circuits containing other elements. The question is: how much redundancy is there? Tellegen discussed a minimum-sized set of elements in 1954 with which *any* linear and non-linear driving-point impedance or transfer characteristic can be synthesised [Tellegen54]. Surprisingly, all but one of the elements are passive. Only one active element is necessary, which we therefore call *the universal active element*. It is the pathological two-port whose input voltage and input current are both zero, irrespective of its output voltage and current.

Anything goes with a universal active element

Zero input current and voltage is what an ideal operational amplifier (opamp) achieves if it is used in a stable feedback configuration. Thus, as we will show later, the opamp is a universal active element. This means that if a suitable set of linear and non-linear passive elements is available, then no active elements other than opamps are needed to implement any linear (e.g. filter) or non-linear (e.g. oscillator) circuit function, as has been demonstrated in several decades of opamp design practice. In this sense, the ideal opamp is *universally versatile*. In the following, we call an amplifier *universal* if its ideal form,

Definition of "universal"

i.e. the amplifier with ideal port impedances and ideal transfer functions, is a universal active element.

Most amplifiers
are universal

It is not difficult at all to find other universal active elements. For example, the current-feedback opamp (CFB opamp), the second-generation current conveyor (CCII−), and the operational transconductance amplifier (OTA) are all universal. Actually, so many universal active elements have been published that most IC designers and circuit theorists have lost track of their development. This is a pity, since having many different universal active elements available is clearly advantageous: Synthesising a circuit *function* on the system level with different amplifiers may result in *systems* with differing numbers of amplifiers and passive components. The properties of the systems, e.g. the sensitivity of system parameters to component value variations, may also come out differently.

Theoretical circuits
and transistor
implementations do
not correspond 1:1

The number of *circuits* approximating the functions of the systems is even larger than the number of systems, since there are always many different ways of implementing a system: The universal active elements can be replaced by circuits approximating them, or sub-blocks of arbitrary complexity can be identified and replaced by circuits that approximately perform the same function. For example, when filters are synthesised using the ideal CCII−, it may happen that one CCII− forms an integrator together with one resistor and one capacitor. Then one can either replace the ideal CCII− by a circuit approximating its function, or one can replace all three elements by an integrator built using a different amplifier, e.g. by a Gm–C integrator containing one OTA and one capacitor. The result may then be the same that could be obtained by synthesising the circuit function using OTAs in the first place.

Naming conventions
are confusing

One more problem for the circuit designer is that the same name, e.g. CCII−, is conventionally used both on the system level for a universal active element and on the circuit level for several different transistor circuits that approximate the ideal CCII−. Furthermore, it frequently happens that a circuit which can be used as an implementation of a certain universal active element is published under a different name. For example, the monolithic nullor in [Huijsing77], the input stage of the CFB opamp in [Analog Devices92], and the transconductance am-

plifier or "ideal transistor" in [Burr Brown95] all approximate ideal current conveyors.

This situation is highly obscure and needs to be clarified. Especially the connection between universal active elements used on the system level and their implementation as integrated circuits needs to be addressed, both to help circuit designers to find the best possible implementation of a system for a specific application and to help system designers who are looking for possible applications of a new integrated amplifier circuit. In order to achieve these goals, we introduce a new classification of universal active elements that provides a direct link between the highly abstract concept of *the* universal active element and integrated-circuit implementations. To provide this link, we will show that the abstract concept of the universal active element fundamentally differs from transistor implementations in two respects: First, the universal active element is defined by *two ports*, whereas the *four terminals* of a transistor circuit can be used independently. Second, the universal active element is defined by its *state*, whereas a transistor circuit implements *controlled sources*. In Section 2.3, the step from two-ports to four-terminals is made. There is a large number of universal four-terminals, but we will identify the two most widespread ones as the *nullor* and the *second-generation current conveyor with negative unity gain (CCII−)*. The next two sections demonstrate the step from state representations to controlled-source representations. In Section 2.4, a set of nine different *operational amplifiers* is derived from the nullor, and twelve different *current conveyors* are derived from the CCII− in Section 2.5. Several of these amplifiers appear to be new, namely the *current-feedback OTA* (CFB OTA) and a whole set of voltage-inverting current conveyors. Finally, we demonstrate in Section 2.6 how *all* amplifiers discussed in this chapter can be implemented in CMOS using a small number of transistor building blocks. To compare like with like, we had to choose one technology. We chose CMOS mainly because we have experience in CMOS amplifier design but not in bipolar amplifier design. This should not affect the generality of our discussion, since the basic operation principles of CMOS and bipolar amplifiers are very similar.

How we intend to clarify this situation

Figure 2.1   *Two-port configurations.*

2.3   Nullors and the universal active element

A two-port description is restricted

As mentioned in the introduction, Tellegen showed that *the universal active element* (he called it "amplificateur idéal," ideal amplifier) has an all-zero chain matrix [Tellegen54],

$$(2.1) \qquad \begin{bmatrix} v_a \\ i_a \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_b \\ -i_b \end{bmatrix},$$

with voltages and currents as defined in Fig. 2.1. Equation (2.1) cannot be used to derive implementations directly, because describing a circuit with four terminals as a two-port means describing it *under the condition that* $i_a = -i'_a$ (see Fig. 2.1). An amplifier with one voltage input and one current input, such as the current-feedback opamp (CFB opamp, see Sec. 2.4 for a definition), cannot operate under this condition, since its voltage input will make $i_a = 0$ and prevent any current from flowing through its current input. For this reason, the CFB opamp has to be treated as a special case in amplifier classifications based on (2.1) [Payne96]. In contrast, a four-terminal classification includes the CFB opamp, as will be shown in Sec. 2.4.

Deriving two four-terminals from Equation (2.1)

The mapping of four-terminals onto two-ports is not one to one, because two-ports are described by two equations, and four-terminal networks by three equations. To derive a universal four-terminal element from (2.1), one equation must be added, which can be chosen freely as long as it does not contradict (2.1). The added equation need not be linear. This means that there is, in theory, an infinite number of qualitatively different universal four-terminal elements. The two simplest and most widespread ones are the *four-terminal nullor* and the *three-terminal nullor*, which were both introduced in [Carlin64].
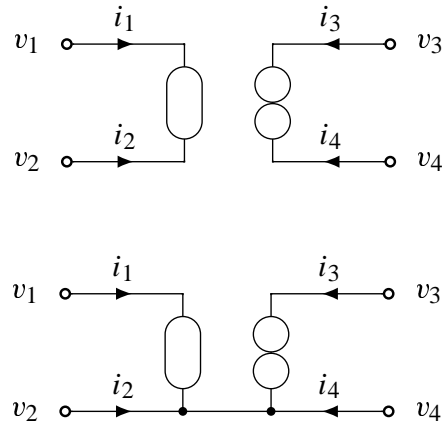
Four-terminal nullor (or simply nullor; top) and three-terminal nullor (CCII−; bottom).

Figure 2.2

The four-terminal nullor consists of two pathological two-terminal elements called *nullator* (terminals 1 and 2) and *norator* (terminals 3 and 4), as shown in Fig. 2.2. The nullator is described by three equations, but the norator only by one:

Description of the nullor

$$\text{(2.2)} \qquad \begin{aligned} \text{Nullator:} \quad & i_1 = -i_2,\ i_1 = 0,\ v_1 - v_2 = 0, \\ \text{Norator:} \quad & i_3 = -i_4 . \end{aligned}$$

The equation $i_3 = -i_4$ makes the nullor fulfil Kirchhoff's current law; $i_1 = -i_2$ is the equation added to (2.1). This means that the four-terminal nullor meets $i_a = -i'_a$, which was discussed above, by itself. Note that it has unfortunately become common practice in the literature to define the four-terminal nullor by (2.1) and then use the device defined by Equation (2.2).

From all universal active elements, the four-terminal nullor is the most straightforward to derive. It has proved to be a very valuable element for network analysis and synthesis (c.f. [Svoboda95] for the analysis of linear circuits, [Hasler95] for non-linear circuits, [Hassoun95] for the nullor's use in CAD software, [Moschytz74, Moschytz75] for the synthesis of linear circuits and filters, [Carlosena93] on nullors and circuit transposition, and [Leuciuc97] on the realization of inverse transfer functions using nullors). We will use the four-terminal nullor in Section 2.4 to derive the nine fundamentally different operational amplifiers.
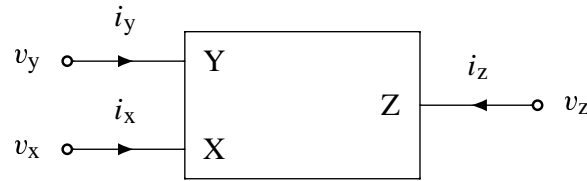
Figure 2.3   *Symbol used for all types of current conveyors.*

The three-terminal nullor is fully equivalent to the four-terminal nullor on the system level, as will be shown presently. It is described by the equations

(2.3) $i_1 = 0,\ v_2 = v_1,\ v_2 = v_4,\ i_3 = -(i_2 + i_4)$.

Here, $i_3 = -(i_2 + i_4)$ describes the Kirchhoff current law, and $v_2 = v_4$ is the equation added to (2.1). The latter equation describes a direct connection between the terminals 2 and 4, which can thus be seen as one terminal, hence the name *three-terminal* nullor. The three-terminal nullor can be represented using one nullator and one norator, i.e. as a four-terminal nullor that has one output connected to one input (c.f. Fig. 2.2). For didactic reasons, we prefer to use an alternative representation of the three-terminal nullor: the second-generation current conveyor with current gain −1, the CCII− [Sedra70, Sedra90], whose circuit symbol is shown in Fig. 2.3. The CCII− is described by three equations,

(2.4) $i_y = 0,\ v_x = v_y,\ i_z = -i_x$,

which are the same as the equations in (2.3), but written in different variables. We will use the CCII− to discuss several current conveyors in Sec. 2.5 and to prove that *all* of them are universal.

For the remainder of this chapter, we will use the name *nullor* for the four-terminal nullor and the name *CCII−* for the three-terminal nullor. Note that the nullor and the CCII− are equivalent on the system level, meaning that any circuit containing only nullors can be re-drawn using only CCII−s, and vice versa. This is easy to show: On the one hand, the CCII− can be drawn using one nullor, as indicated by Fig. 2.2, and one way to actually implement a CCII− is in fact to connect two terminals of a nullor implementation

(c.f. Section 2.6). On the other hand, a nullor can simply be re-drawn by using two CCII−s and connecting their X terminals, and one way to implement a four-terminal nullor is to connect the X terminals of two CCII− implementations [Cabeza94, Cabeza97, Payne96].

Operational amplifiers 2.4

In electronics textbooks, the conventional operational amplifier is often described by two rules: (i) the output attempts to do whatever is necessary to make the voltage difference between the inputs zero, and (ii) the inputs draw no current. These rules are called the "Two Golden Opamp Rules" in [Horowitz89]. They both contain the information of the nullator equations in (2.2) and the statement that feedback is necessary such that the opamp can approximate the nullator equations. Thus we call an amplifier *operational* if it can approximate the nullor in certain feedback configurations. It follows directly from this definition that all operational amplifiers are universal. It will become apparent in the forthcoming discussion that our definition of "operational" agrees closely with the common sense of amplifier designers. (Originally, the name "operational" was given to these amplifiers because they could be used to implement mathematical operations, e.g. integrations.)

Definition of "operational"

The nullor cannot be implemented in a straightforward way. Being described by its state only, its terminal impedances are undefined, whereas the terminal impedances of an ideal amplifier are either zero (low) or infinite (high). There are three different ways of choosing the impedances of the input terminals: both low, both high, or one low and one high. The same applies to the outputs. Therefore there exist nine fundamentally different operational amplifiers, described by Tab. 2.1, whose circuit symbols are shown in Fig. 2.4.

Nine ways of choosing terminal impedances

The nine operational amplifiers are ordered according to their input and output stages in Fig. 2.4. The three rows of Fig. 2.4 contain the amplifiers with voltage ($\mathbb{V}$), current ($\mathbb{I}$), and hybrid ($\mathbb{H}$) input stages, and the three columns contain the amplifiers with $\mathbb{I}$, $\mathbb{V}$, and $\mathbb{H}$ output stages (we will presently describe all stages). The names of the various amplifiers are listed

The naming of operational amplifiers

Class	Gain Equation	Operational for	Common Name
V–I	$i_3 = g_m(v_1 - v_2)$	$g_m R_{in} \to \infty$	operational transconductance amplifier (OTA)
V–V	$v_3 = A_v(v_1 - v_2)$	$A_v \to \infty$	operational amplifier (opamp)
V–H	$v_3 = A_v(v_1 - v_2)$	$A_v \to \infty$	floating opamp (operational floating amplifier, OFA)
I–I	$i_3 = A_i i_1$	$A_i \to \infty$	current-mode opamp
I–V	$v_3 = r_m i_1$	$r_m/R_{in} \to \infty$	operational transresistance amplifier (OTRA)
I–H	$v_3 = r_m i_1$	$r_m/R_{in} \to \infty$	floating OTRA
H–I	$i_3 = A_i i_2$	$A_i \to \infty$	current-feedback OTA (CFB OTA)[†]
H–V	$v_3 = r_m i_2$	$r_m/R_{in} \to \infty$	current-feedback opamp (CFB opamp)
H–H	$v_3 = r_m i_2$	$r_m/R_{in} \to \infty$	operational floating conveyor (OFC)

Table 2.1: *Common names of the nine operational amplifiers ([†]this name is proposed by us).*
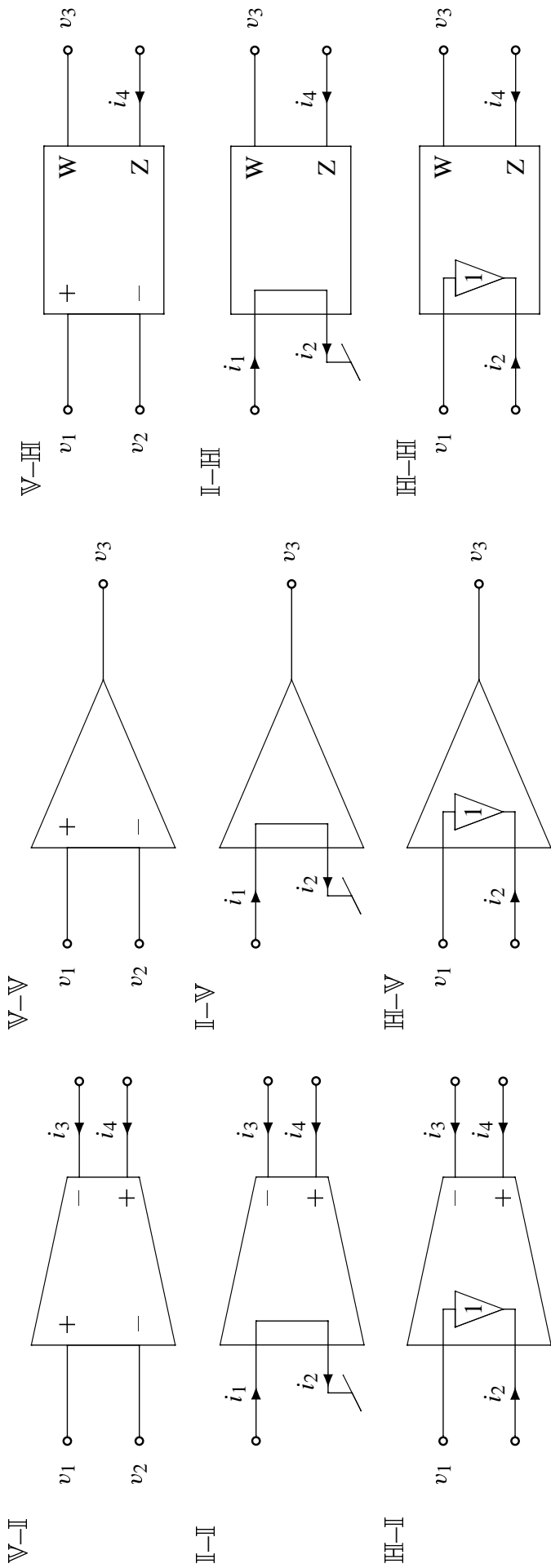
Figure 2.4: *Symbols of the nine operational amplifiers.*

in Tab. 2.1. All amplifiers have already been named in the literature, with the exception of the $\mathbb{H}$–$\mathbb{I}$ amplifier, which we call *current-feedback OTA* (CFB OTA) because its relation to the OTA is the same as the CFB opamp's relation to the opamp. Both names are misleading, since the CFB OTA is actually a current amplifier and not a transconductance amplifier, just as the CFB opamp is a transresistance amplifier and not a voltage amplifier. We decided to use the name CFB OTA anyway to preserve some symmetry in the nomenclature. In a perfectly symmetrical nomenclature, the $\mathbb{H}$–$\mathbb{H}$ amplifier would be called floating CFB opamp; however, to remain consistent with the literature, we prefer to use its conventional name, operational floating conveyor (OFC) [Payne91, Toumazou93].

High-gain stages are not always necessary

Table 2.1 also contains the gain equations of the amplifiers and the conditions under which the amplifiers are operational in a feedback configuration. These conditions will be derived presently. Table 2.1 states that the four amplifiers with voltage gain or current gain are only operational if their gains A_v and A_i are very high. These four amplifiers need a high-gain stage between the input and the output stage (see Sec. 2.6). This is not the case for the OTA. If one output terminal is directly connected to one input terminal, the loop gain becomes $g_\mathrm{m} \cdot R_\mathrm{in}$, where g_m and R_in are the OTA's transconductance and input resistance. Integrated OTAs normally have a very high input resistance, so an OTA is operational even if its g_m is low. Similarly, if direct feedback is applied to any of the four transresistance amplifiers, the feedback loop has a gain of $r_\mathrm{m}/R_\mathrm{in}$. Looking at integrated circuits again, one finds that it is difficult to make R_in very low. Thus many implementations of such transresistance amplifiers, most notably implementations of CFB opamps, do contain a high-gain stage which makes the transresistance r_m very high.

Voltage, current, and hybrid input stages

We will now show how the set of nine operational amplifiers can be derived from the nullor equations (2.2). If the input stage is identified with the nullator and the output stage with the norator, it becomes apparent that the input stage is over-defined by the three nullator equations, whereas the output stage is under-defined by the single norator equation. The principle underlying all nine operational amplifiers is that the output stage fulfils one additional equation, a gain equation, which enables the amplifier to satisfy all three nullator equations

if it is used in a stable infinite-gain feedback configuration.
Choosing the nullator equation to be satisfied by feedback
determines both the type of the input stage and the quantity
to be amplified. There are three possible choices: **(i)** Satisfy
$v_1 - v_2 = 0$ by feedback. Then $v_1 - v_2$ must be amplified, and
the input stage must fulfil the nullator equations $i_1 = 0$ and
$i_1 = -i_2$ by itself. Substituting the former equation into the
latter results in $i_2 = 0$, thus both terminals must have a high
impedance. This describes the $\mathbb{V}$ input stage. **(ii)** Satisfy $i_1 = 0$
by feedback. The input stage must then meet $i_1 = -i_2$ and
$v_1 - v_2 = 0$, which describes a short circuit. Because $i_1 = -i_2$,
either i_2 or i_1 can be amplified. In Fig. 2.4, all $\mathbb{I}$ input stages
are shown with one of the inputs grounded, because integrated
$\mathbb{I}$ input stages normally have only one current input. More is
not necessary; an $\mathbb{I}$-input amplifier is still universal if it has
only one input terminal, since the current-adding capability
of the current input makes it possible to use the single $\mathbb{I}$ input
terminal both for applying the feedback necessary to force
$i_1 = 0$ and to transport a signal current. The only difficulty is
that a synthesis technique different from conventional nullator-
norator synthesis must then be used to ensure that no floating
nullators occur in the system. **(iii)** Satisfy $i_1 = -i_2$ by feedback.
The equations fulfilled by the input stage are then $i_1 = 0$ and
$v_1 - v_2 = 0$, and the signal to be amplified is i_2. Thus terminal 1
must have high impedance, terminal 2 low impedance, and the
voltage from terminal 1 must be replicated at terminal 2. This
is the $\mathbb{H}$ input stage, which has become well known through
the CFB opamp. The $\mathbb{H}$ input stage can also be understood as
an extended $\mathbb{I}$ input stage whose analogue ground voltage is
not fixed, but can be set through an additional terminal. We
will show in Sec. 2.6 that many current input stages can easily
be used as hybrid stages, simply by using a circuit node that
was formerly connected to analogue ground as an additional
voltage input terminal.

The output signal of an amplifier can either be a voltage
or a current. This choice and the choice of the input stage
determine the amplifier's gain equation. The output stage must
also meet the single norator equation $i_3 = -i_4$. There are
again three possibilities: **(i)** An $\mathbb{I}$ output stage just requires two
balanced current outputs. **(ii)** Building a $\mathbb{V}$ output stage that
fulfils $i_3 = -i_4$ means building a floating controlled voltage
source with invertible polarity. Fortunately, doing this is not

necessary, since only one voltage output is really needed. The voltage-fan-out capability of the $\mathbb{V}$ output makes it possible to drive the feedback and deliver an output signal simultaneously. Thus integrated $\mathbb{V}$ output stages normally have only one output voltage, which is reflected in the symbols used in Fig. 2.4. **(iii)** Like the $\mathbb{I}$ input stage, the $\mathbb{V}$ output can also be extended to a hybrid stage. Since the hybrid output stage must meet $i_3 = -i_4$, it must copy the current flowing into the voltage output terminal to an additional current output terminal. This technique, which is called *output current sensing* or *supply current sensing*, will play an important role in the following two sections. In Fig. 2.4, we denote the voltage output terminal of the $\mathbb{H}$ output stage by W and the current output terminal by Z, a convention taken from the symbol normally used for the OFC [Payne91, Toumazou93].

How to extend operational amplifiers
Fig. 2.4 does not show some special types of amplifiers, like differencing-input current amplifiers [Mucha95, Mucha96], differential difference amplifiers [Säckinger87], or balanced-output opamps [Banu85]. This is because, e.g., a balanced voltage output stage cannot be described as a single $\mathbb{V}$ output stage fulfilling the gain equation and the norator equation. The balanced-output opamp must rather be seen as an *extended* voltage opamp, a voltage opamp that has an additional voltage output stage. Similarly, the differential difference amplifier has an additional pair of voltage inputs, and the differencing-input current amplifier has an additional current input. All extended amplifiers are trivially universal, since one can just leave the additional inputs or outputs unused to get one of the amplifiers in Fig. 2.4. It now becomes apparent that any number of universal active elements can be constructed from the ones in Fig. 2.4, which is the main reason why new universal amplifiers are still published now and then.

2.5   Current conveyors

How to prove that a current conveyor is universal
In the previous section, nine operational amplifiers that fulfil the nullor equations were derived. We will now use the CCII− to discuss several current conveyors. They do *not* meet the CCII− equations (2.4) but are still universal. It could be shown mathematically that every one of these current conveyors is
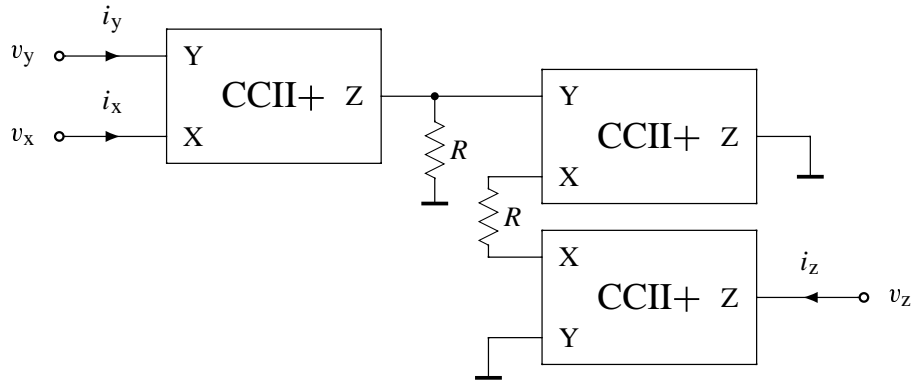
CCII− built using three CCII+ and two resistors. **Figure 2.5**

universal, but we will pursue a more intuitive approach: we will show for every current conveyor that, on the system level, the CCII− can be replaced by a network containing only resistors and one or more instances of the current conveyor in question.

In contrast to the nullor, the CCII− can be implemented directly and does not require a high-gain stage. The three equations in (2.4) can be interpreted as a description of two interlinked controlled sources: $i_y = 0$ states that Y's terminal impedance is high. $v_x = v_y$ can be interpreted as a voltage buffer from terminal Y to terminal X. Under this interpretation, $i_z = -i_x$ states that the current flowing into the output of the voltage buffer is sensed and copied to terminal Z, which therefore has high impedance. This sounds familiar, since the sensing of the current flowing into a voltage output is used both in the $\mathbb{H}$ input stage and the $\mathbb{H}$ output stage discussed in the previous section. We will show in the following section that the two are indeed current conveyors. Note that current sensing applied to a voltage buffer is only one possible interpretation of the CCII− equations, the other important interpretation was already mentioned in Sec. 2.3 and describes the CCII− as a nullor with one output connected to one input.

Describing the CCII− as two interlinked, controlled sources

A different current conveyor results if $i_z = -i_x$ is replaced by $i_z = +i_x$: the *CCII+* [Sedra70, Sedra90]. The CCII+ is not a true three-terminal network anymore, since its terminals do not meet Kirchhoff's current law. Like the opamp, it must rather be seen as a four-terminal network of which one terminal is not accessible to the user. To prove that the CCII+ is universal, it is sufficient to show that a CCII− can be replaced by a

CCII+: positive current gain

circuit consisting of three CCII+ and two resistors with equal resistance. Such a circuit is shown in Fig. 2.5.

In general, the CCII with positive or negative current gain α_i is described by the current equation $i_z = \alpha_i i_x$ [Schmid97, Schmid99b]. It is universal for any non-zero α_i. To prove this for positive α_i, it suffices to show that the circuit in Fig. 2.5 is a CCII− if the two resistances are chosen such that the overall current gain becomes one. The same circuit can also be used to prove universality for negative α_i: just use the Z terminal of the top right CCII as the output of the composite CCII−. (The bottom right CCII can then be omitted.)

The CCII was originally derived from a device introduced as "the current conveyor," which is now called *first-generation current conveyor*, or CCI+. The CCI+ is described by the following three equations [Smith68]:

$$(2.5) \qquad i_y = i_x, \; v_x = v_y, \; i_z = i_x \, .$$

To prove that it is universal, it is sufficient to show that a CCII− can be built using two instances of the CCI+. One way to do this is shown in Fig. 2.6. Defining $i_x = I$ and drawing this current I wherever it occurs makes it obvious that the circuit in Fig. 2.6 meets Eqs. (2.4) and thus is a CCII−. Other current conveyors similar to the CCI+ are the CCI− ($i_z = -i_x$), the CCIα_i ($i_z = \alpha_i i_x$), and the third-generation current conveyor, CCIII ($i_y = -i_x$, c.f. [Fabre95]), or, more generally, the CCIIIα_i. All first- and third-generation current conveyors are universal amplifiers, which can in every case be shown by a constructive proof, as for the CCII+ and the CCI+. Finally, it is also possible to choose a non-unity current gain from X to Y, i.e., to choose $i_y = \pm\alpha_j i_x$. The resulting amplifier is universal for any α_j.

A further idea is to use a voltage inverter instead of a voltage buffer at the input of any of these current conveyors, such that $v_x = -v_y$. It is not clear yet what kind of applications current conveyors containing a voltage inverter may have, we only include this case for the sake of completeness, and also because this functionality was used to build a filter (but not explicitly described) in [Chiu96, Fig. 10]. We propose the name *voltage-inverting current conveyor* (VICC) for such devices. Current conveyors of all three generations can be built
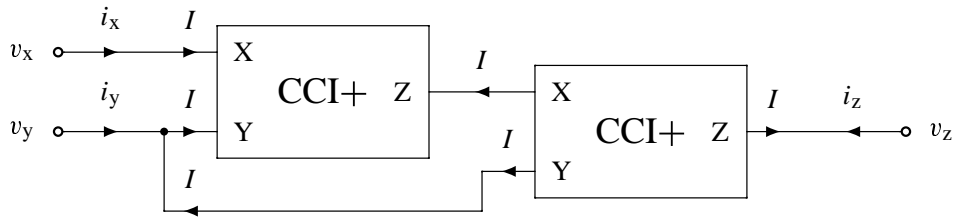
CCII− built using two CCI+.   **Figure 2.6**

with a voltage inverter, thus there exist VICCIs, VICCIIs and VICCIIIs. All are universal, since two VICCs can be used to build one normal current conveyor, namely by using its voltage inverter to convert the inverting Y terminal to a non-inverting one. Note that using two VICCIs or two VICCIIIs gives a CCIII, whereas two VICCIIs give a CCII. Further research will show whether the VICCs are actually useful for network synthesis.

It depends on the viewpoint how many different current conveyors our classification contains. If non-unity gains are just seen as a generalisation of a given current conveyor, then there exist twelve different current conveyors named according to the scheme *xCCyz*, where *x* is either "VI" or nothing to denote the polarity of the voltage buffer, *y* is either "I", "II", or "III" to denote the polarity or the absence of a Y-terminal current, and *z* is "+" or "−" to denote the polarity of the output current buffer.

Twelve classes of current conveyors

More universal amplifiers based on these twelve current conveyors can be derived by adding more current inputs and outputs (c.f. the balanced-signal CCII in [Schmid97, Schmid99b]) or more voltage inputs (c.f. the differential difference CCII in [Chiu96]). Like the extended operational amplifiers from Sec. 2.4, they are all trivially universal.

Extended current conveyors
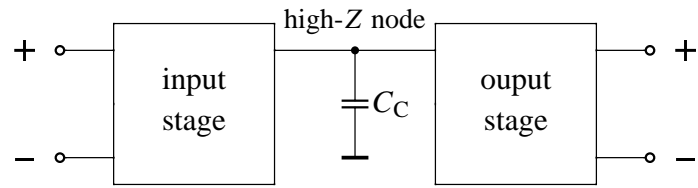
Figure 2.7   *Block diagram of an operational amplifier.*

	input stage	output stage
$\mathbb{V}$	single-ended OTA	voltage buffer
$\mathbb{I}$	current buffer	balanced-output OTA
$\mathbb{H}$	CCII±	CCII−

Table 2.2   *Functions of the opamp stages.*

2.6   Implementation in CMOS

The six stages
needed to build
operational amplifiers

All operational amplifiers besides the OTA are normally im-
plemented as an input stage and an output stage connected by
a compensated high-impedance node. The simplest compen-
sation circuit, shown in Fig. 2.7, is a compensation capacitor
C_C between the high-impedance node and ground. More
elaborate compensation schemes use local feedback to reduce
the size of the compensation capacitor [Johns97, Laker94].
The circuit that is dual to a capacitively compensated high-
impedance node is a compensation inductor connecting two
low-impedance nodes (as in [Carlosena94, Fig. 3]), but it is sel-
dom used because of the lack of very low terminal impedances
and high-Q inductors on integrated circuits. Thus all opamp
input stages must have a current output, and all opamp output
stages must have a voltage input. The functions that have to be
performed by the stages discussed in Sec. 2.4 can now easily be
determined; they are listed in Table 2.2. The required building
blocks are therefore a single-ended OTA, a balanced-output
OTA, a voltage buffer, a current buffer, a CCII+ and a CCII−;
thus we will start this section with discussing implementations
of OTAs and of the twelve current conveyors classified in the
previous section.

CMOS OTAs

All six stages can be shown in only three figures, Figs. 2.8–
2.10, since the voltage buffer and the current buffer are already
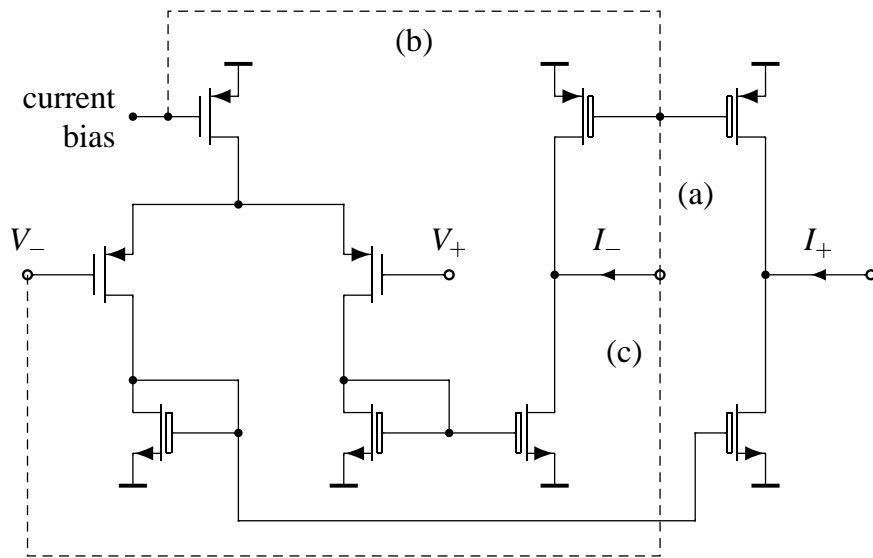
Single-output OTA (if connection (a) is made),
balanced-output OTA (if connection (b) is made),
and OTA-based CCII− (if both connections
(b) and (c) are made).

Figure 2.8
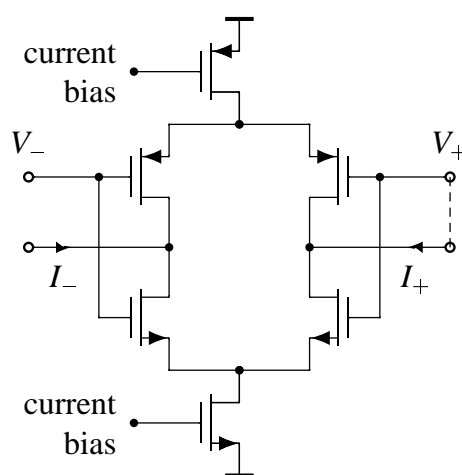
Balanced-output OTA (or floating current source),
and OTA-based CCII− (if the dashed connection is made).

Figure 2.9
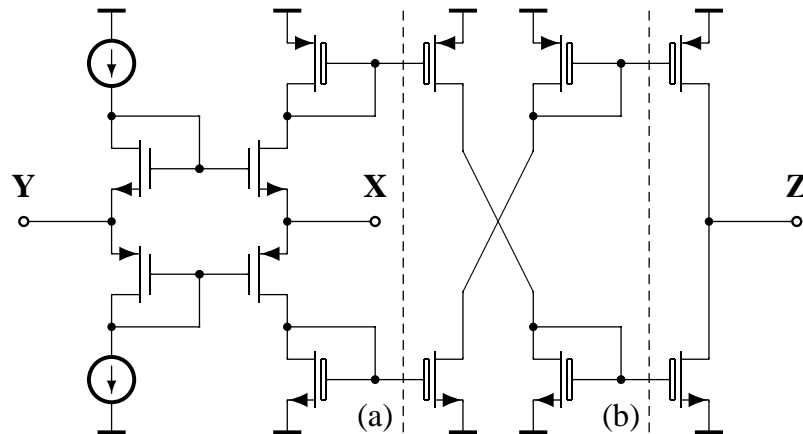
Figure 2.10   *CCII−, CCII+ (if the part between (a) and (b) is omitted),*
current buffer (if Y is connected to analogue ground),
and voltage buffer (if everything right of (a) and the two
diode-connected transistors just left of (a) are omitted).

parts of the CCII shown in Fig. 2.10: to use that CCII as a
voltage buffer, one can simply omit the output-current-sensing
circuitry, and to use it as a current buffer, its Y terminal must
be connected to analogue ground. Note that most current input
stages are actually built in this way. The input stage of every
voltage opamp is an OTA, thus this device is well known. The
differential-pair structure shown in Fig. 2.8 is conventionally
called current-mirror OTA [Johns97, Laker94]. The transistors
having boxes as gates are composite transistors with high
output resistance, e.g. normal cascodes, low-voltage cascodes,
or regulated cascodes (c.f. [Johns97, Wang90, Säckinger90]).
The OTA structure shown in Fig. 2.8 can be used to implement
both a single-ended OTA and a balanced-output OTA. The
latter is already an implementation of the $\mathbb{V}$–$\mathbb{I}$ operational
amplifier, as discussed in Sec. 2.4. It could also be used
as a balanced current output stage, but many designers (e.g.
[Mucha95]) have started to use the OTA shown in Fig. 2.9. This
OTA is called *floating current source* [Arbel92] and essentially
consist of two differential pairs connected head to head. The
advantage of this simple structure is that the relation $I_+ = -I_-$
is guaranteed by Kirchhoff's current law and is therefore very
precise and very linear, whereas in the OTA in Fig. 2.8, the
precision of that relation depends on how well the two output
current mirrors match.
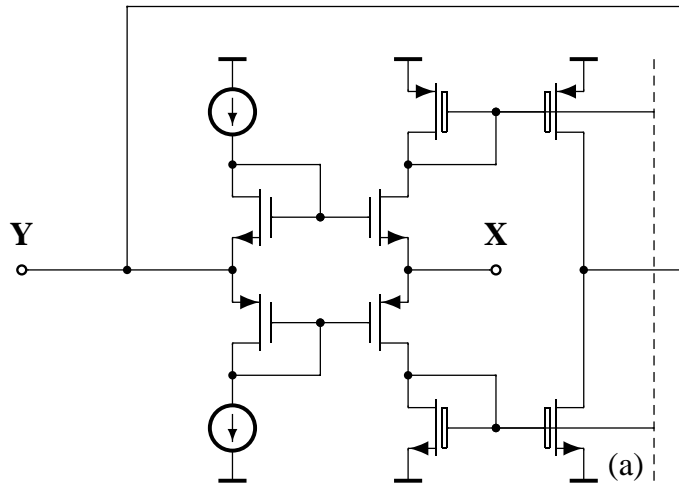
Input circuit of a CCI. **Figure 2.11**

We already showed in Sec. 2.3 that a CCII− results if one of the outputs of a balanced-output OTA is connected to one of its inputs. This can be done with both OTAs discussed above. An alternative way of implementing the CCII− as a class-AB circuit is as a voltage buffer with output-current sensing, shown in Fig. 2.10 [Lidgey94]. In contrast to an OTA with feedback, the circuit in Fig. 2.10 can easily be altered to obtain a CCII+: omit the current inverter between the dashed lines in Fig. 2.10. This stage is often preferred as an $\mathbb{H}$ input stage, mainly because using a CCII− is not really an option, which we will show presently when we discuss the CFB opamp. But first we briefly explain how these circuits can be used to implement the twelve classes of current conveyors.

*CMOS CCII−
and CCII+*

A CCIIα_i can be built by taking the CCII+ or CCII− implementation in Fig. 2.10 and re-sizing some of the current mirror transistors. All CCIIs can be converted to CCIs if the voltage buffer left of the dashed line (a) is replaced by the the circuit in Fig. 2.11 [Bruun95]. CCIIIs can be built in much the same way, by simply using one more current inverter in Fig. 2.11, although they were implemented using two double-output CCIIs when they were first proposed [Fabre95]. Like the CCII, CCIs or CCIIIs with non-unity gain can be built by re-sizing some of the current mirror transistors.

*CMOS CCIIα_i, CCI
and CCIII*

Voltage-inverting current conveyors require a voltage inverter between Y an Z. This can be achieved by using the two-differential-pair input stage of the differential difference

CMOS VICCs
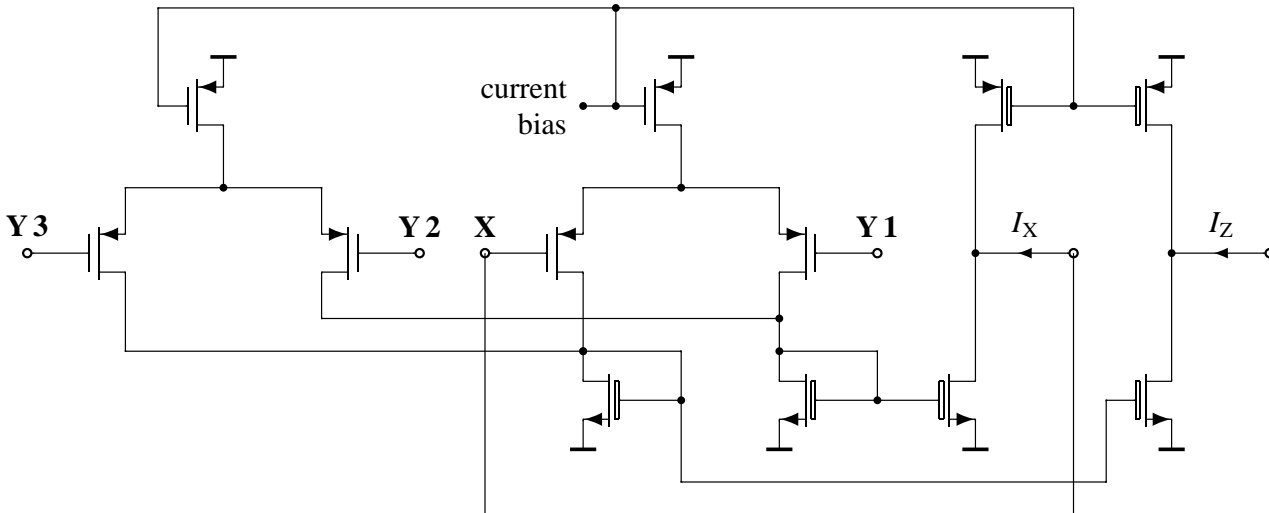
Figure 2.12   *Current conveyor with a differential difference input stage.*

amplifier [Säckinger87] instead of a conventional OTA (c.f. [Chiu96]). If this technique is applied to the OTA in Fig. 2.8, then the circuit in Fig. 2.12 results. The voltage at X is $V_X = V_{Y1} + V_{Y2} - V_{Y3}$, thus a VICCII+ results if both Y 1 and Y 2 are connected to ground. All other VICCs can be built based on this VICCII+ by adding current mirrors and current inverters.

Extended current conveyors and class-A current conveyors

Finally, extended current conveyors, such as multiple-output current conveyors or balanced-signal current conveyors, can be built by replicating parts of the circuits in Figs. 2.10 and 2.11 [Schmid97, Schmid99b, Schmid00d]. Many of these current conveyors can also be built as class-A circuits instead of class-AB circuits [Lidgey94, Schmid99b, Schmid00d], as in Chap. 6.

Brief discussion of the nine operational amplifiers

All stages necessary to build the operational amplifiers from Sec. 2.4 are now described. The following comments on each amplifier explain a few important design considerations and briefly describe other notable implementations of the nine operational amplifiers.

$\mathbb{V}$–$\mathbb{I}$

The OTA ($\mathbb{V}$–$\mathbb{I}$ amplifier) is normally built without an internal high-impedance node, since it is operational even if its transconductance is not high (see Sec. 2.4). This makes it possible, in the extreme case, to build a CMOS OTA that only has input and output nodes, but no internal nodes at all [Nauta92]. Note that an OTA need not even be operational if it is used to

build transconductance–C (Gm–C) filters. Nevertheless, there
are OTAs having an internal high-impedance node, most no-
tably the "monolithic nullor" proposed in [Huijsing77], which
is built as a cascade of two bipolar differential pairs.

Voltage opamps ($\mathbb{V}$–$\mathbb{V}$ amplifiers) often contain a voltage $\mathbb{V}$–$\mathbb{V}$
buffer different from the one in Fig. 2.10, and most opamps
are compensated by an internal feedback capacitor [Johns97,
Laker94] instead of a grounded capacitor.

The floating opamp ($\mathbb{V}$–$\mathbb{H}$ amplifier, also called operational $\mathbb{V}$–$\mathbb{H}$
floating amplifier) uses a CCII− as its output stage. As
explained above, it can be seen as an extended voltage opamp
whose output current is sensed and mirrored to another output.
Most output stages used in CMOS and bipolar opamps can
be modified in this way. It is also possible to sense and copy
the supply currents of the whole opamp, since any current
flowing into the opamp's output must flow through the opamp's
supplies. Thus off-the-shelf discrete opamps can be made
floating by adding external current mirrors, as discussed in
[Huijsing90].

The CFB opamp ($\mathbb{H}$–$\mathbb{V}$ amplifier) has become famous through $\mathbb{H}$–$\mathbb{V}$
its gain-independent bandwidth (c.f. [Bruun93, Bowers93,
Franco93, Harvey93, Toumazou93] and the discussion in
Sec. 3.4.3). Both the CCII− and the CCII+ could be used as
its input stage, but the latter is preferable. If a CCII+ is used,
external negative feedback goes from the output to the current
input, which is then called the negative input, and the positive
input can be used to feed a voltage signal into the feedback
loop. However, if a CCII− were used, a negative feedback
loop would go through both the voltage and the current buffer
of the $\mathbb{H}$ input stage. The feedback signal would then again be
a voltage, and the resulting $\mathbb{H}$–$\mathbb{V}$ opamp would be slower and
would not have a gain-independent bandwidth anymore. Thus
CFB opamps almost always have a CCII+ input stage. For
example, the AD 844 CFB opamp [Analog Devices92] has a
structure very similar to the structure presented here, although
bipolar transistors are used. The AD 844 is special in that its
internal high-impedance node is available as a chip pin. Thus
its input stage can be used as an independent CCII+, which is
often done to build CCII+ circuits with discrete components
[Svoboda91].

$\mathbb{H}$–$\mathbb{H}$ **The OFC** ($\mathbb{H}$–$\mathbb{H}$ amplifier) can be seen as a floating CFB opamp. The $\mathbb{H}$–$\mathbb{H}$ structure implemented here is similar to the bipolar-transistor OFC described in [Payne91, Toumazou93]. The OFC is basically a transresistance amplifier, as its gain equation shows.

$\mathbb{I}$–$\mathbb{V}$ **OTRAs** ($\mathbb{I}$–$\mathbb{V}$ amplifiers) are only occasionally used in the literature. The OTRA developed for transresistance–C filters that was presented in [Lu94] is very similar to the one described here, but normally OTRAs are used for special purposes only and are then implemented in special ways (c.f. [Wulleman97]). As explained above, most amplifiers with $\mathbb{I}$ input stages are already full-grown $\mathbb{H}$-input amplifiers with their voltage input grounded. This is also true for the OTRA in [Lu94], which can thus very easily be converted into a CFB opamp.

$\mathbb{I}$–$\mathbb{H}$ **The floating OTRA** ($\mathbb{I}$–$\mathbb{H}$ amplifier) can be used to couple current signals out of the loop of a transresistance–C filter, e.g., to make the filters from [Lu94] more versatile. The relation between the OFC and the floating OTRA is the same as the relation between the CFB opamp and the OTRA. Thus any of the latter three can be interpreted as an OFC with one or two grounded terminals. Fast CMOS floating OTRAs have already been published under the name "current-mode opamp" [Kaulberg93, Palmisano98] and "transresistance current amplifier" [Palmisano97].

$\mathbb{I}$–$\mathbb{I}$ **The current-mode opamp** ($\mathbb{I}$–$\mathbb{I}$ amplifier) in [Mucha95] uses the CCII+ from Fig. 2.10 as its input stage and the floating current source from Fig. 2.9 as its output stage.

$\mathbb{H}$–$\mathbb{I}$ **The CFB OTA** ($\mathbb{H}$–$\mathbb{I}$ amplifier) was, to our knowledge, not discussed in the literature before, but it can easily be built from most current-mode opamp circuits, just as a CFB opamp can be built from an OTRA. To explain what it can be used for, a brief excursion to circuit transposition is necessary.

Transposition and duality of operational amplifiers   If a linear voltage-mode circuit is *transposed*, a current-mode circuit results that has the same transfer function. When a circuit is transposed, the output terminals become the input terminals, and vice versa, but the terminal impedances remain the same. The transposed circuit is also called the *dual* circuit. The passive part of a linear circuit remains the same under circuit transposition, only the active devices
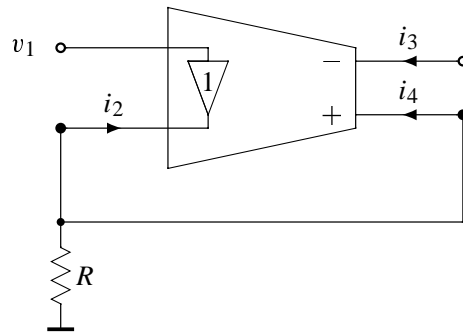
Highly linear voltage to current converter.   **Figure 2.13**

must be exchanged, and the signal flow must be reversed (c.f. Section 3.3, [Bhattacharyya71, Moschytz94, Roberts92, Roberts90]). It can be shown that the $\mathbb{I}$ input stage is dual to the $\mathbb{V}$ output stage, the $\mathbb{V}$ input stage is dual to the $\mathbb{I}$ output stage, and the $\mathbb{H}$ input stage is dual to the $\mathbb{H}$ output stage. Thus three of the nine opamps are self-dual: the $\mathbb{V}$–$\mathbb{I}$ amplifier, the $\mathbb{I}$–$\mathbb{V}$ amplifier, and the $\mathbb{H}$–$\mathbb{H}$ amplifier. This means, for example, that the transpose of a voltage-mode Gm–C filter is a current-mode Gm–C filter, and that the transpose of a voltage-to-current converter still is a voltage-to-current converter. Note that the three self-dual operational amplifiers lie on one diagonal in Fig. 2.4. Transposing all amplifiers in Fig. 2.4 amounts to mirroring the figure at this diagonal.

Now the use of the CFB OTA is apparent: since it is dual to the $\mathbb{V}$–$\mathbb{H}$ amplifier, it can be used to transpose any circuit containing floating opamps. To give a simple example for the potential of the CFB OTA, a voltage-to-current converter is shown in Fig. 2.13. It is the dual of a floating-opamp voltage-to-current converter presented in [Huijsing90]. Compared to the latter, the CFB OTA circuit has two main advantages: First, it is easier to implement. As explained above, most current opamps can be used as CFB OTAs without adding a single transistor, whereas converting a voltage opamp into a floating opamp requires adding several current mirrors. Second, the CFB OTA circuit is more linear: Its harmonic distortion is mainly caused by the nonlinear output of the $\mathbb{H}$ input voltage buffer. Since current feedback is used, i_2 is very low, and the buffer may consequently be very linear. If the $\mathbb{I}$ output stage is a floating current source, then the output current i_3 contains as little distortion as the feedback loop current i_4, since the two

On the use of the
CFB OTA

are related by Kirchhoff's current law. In contrast, the current output of the floating-opamp voltage-to-current converter is the mirrored terminal current of the floating opamp's voltage output. Thus the achievable linearity is limited by the current mirrors in the $\mathbb{H}$ output stage.

2.7   Conclusion

A new amplifier classification

The classification of universal amplifiers presented in this chapter places all operational amplifiers and current conveyors known from the literature into a common framework, together with abstract concepts such as the universal active element and the nullor. We demonstrated how closely our classification is related to the way amplifiers are integrated by showing that all of them can be implemented in CMOS using only a few basic circuits. Although we only discussed CMOS, our classification applies to bipolar amplifiers as well, because the voltage buffers, current mirrors, and long-tailed pairs used in this chapter can also be integrated with bipolar transistors.

Several new amplifiers

In this chapter, several universal active elements appeared that were not previously published. On the one hand, it occurred that first-, second- and third-generation current conveyors still are universal if voltage inverters instead of voltage buffers are used as their input stages. The potential of these voltage-inverting current conveyors will be the topic of future research. On the other hand, a new operational amplifier, the *current-feedback OTA* (CFB OTA), was briefly discussed. It is dual to the floating opamp, but can be built from most current opamps without adding a single transistor. As an example, a voltage-to-current converter containing one CFB OTA and one resistor was discussed.

Use of the classification

Our classification may be useful in different ways. Because of its close relation to IC design, it should give the reader some insight into the similarities between different integrated amplifiers, such that when they encounter an amplifier they have not seen before, they can quickly see what it does and also how it is related to the amplifiers they are already familiar with. It may also help IC designers to understand the relevance of a newly introduced circuit-theoretical amplifier concept and enable

them to find out in which way it should best be implemented for a certain application. From a purely theoretical point of view, and as far as we know, our classification is the most extensive of all recently published amplifier classifications, although it has comparable complexity.

This chapter has also shown that all broad-band amplifiers which have been introduced in the past few decades and have been described as very versatile are in fact *universally* versatile, which means that *every* linear and non-linear circuit function can be built from multiple instances of any one of these amplifiers and a set of linear and non-linear passive components. Neither of these amplifiers is more or less versatile than the others, although they require different synthesis methods.

The abundance of universally versatile amplifiers

The main question that is left open is: How should a designer choose the best amplifier for a certain application? We deliberately left this question open, because we do not think that a simple answer exists. The opamp, the CFB opamp and the OTA are well known by now, but comparatively little research has been done about the other universal amplifiers. So, at least at present, a designer should probably best choose the kind of amplifier which he knows best or about which he can gather sufficient knowledge from other people, and then optimise this amplifier with respect to the application.

Open questions

Chapter 3

Current-mode and voltage-mode filters

See first, think later, then test.
But always see first.
Otherwise you will only see
what you were expecting.

(Douglas Adams)

In this chapter, the current-mode vs. voltage-mode debate is taken up again using the notion of driving-point impedances. First, the nature of the common definitions of the current mode and of the performance statements found in the basic papers on current-mode techniques are discussed. Then a new proof of the circuit transposition theorem is presented that has the advantage of being intuitive for today's engineers and students and thus makes the use of transposition tables unnecessary. Finally, several cases are discussed in which current-mode and voltage-mode circuits have different performance, and it is shown in every case that the reason for the performance difference is not the mode of the signal.

3.1   Background

Discussing the difference between filters containing volt-
age opamps and filters containing current opamps was the
first task I was given when I started my doctoral studies.
I soon deviated from this task, because I simply failed to
find any relevant theoretical differences, and started to
investigate into single-current-conveyor biquadratic filters.

I was pushed back into the current-mode vs. voltage-mode
debate several times during my time as a doctoral student,
sometimes when reading a paper, sometimes when talking
to people who know the current-mode community. Espe-
cially my discussions with Markus Helfenstein on the
subject brought me to the point where I started to believe
that there is no real difference between current-mode and
voltage-mode circuits.

So I tried to prove that there is no real difference, only to
find out that I could not do it, mainly because I could not
find a strict definition of voltage mode and current mode.
There are several definitions in the literature, but either
they are too unprecise to be used for a formal proof, or
they are too restrictive to be acceptable representations of
current mode and voltage mode as they are understood by
the circuit designers involved in the debate.

This chapter is my attempt to support the view that the
current-mode way of thinking [Toumazou90] is a pow-
erful concept that broadened the horizon of IC design,
but cannot be used to make a sharp divide between two
classes of circuits having different performance properties.
I decided long ago to explain all this in terms of node
impedance, a view I inherited from Bram Nauta during
a personal discussion at the AACD 1998 in Copenhagen.

Then I found Ochoa's paper about driving-point signal-
flow graphs [Ochoa98], which gave me the tool to prove
the circuit transposition theorem in terms of node imped-
ances. I did this for very personal reasons: I had great
difficulties to understand the original proofs for network
transposition, since I knew too little about abstract net-
work theory as it was used 30 years ago. Most students

and engineers are in the same situation, but many know signal-flow graphs, so I decided to re-formulate the theory using driving-point signal-flow graphs. The result now forms the middle section of this chapter.

Current mode and voltage mode in the literature
<div style="text-align:right">3.2</div>

Originally, the term "current mode processing" was coined by Barrie Gilbert when he worked on strict trans-linear loops (c.f. [Toumazou90]), in which the voltages truly are incidental.[1] Nowadays we are persuaded that current-mode integrators, filters, and oscillators have some special merit. But is this really true? In contrast to strict trans-linear loops, these circuits rely on an intimate dialogue between voltage signals and current signals.

Origin of "current mode"

When comparing current-mode to voltage-mode filters, one should perhaps first ask two questions:

Two important questions

1. Are there any definitions of current mode that make a clear divide between voltage-mode and current-mode circuits?

   We will call this a *precise* definition from here on.

2. Is it necessary to have a precise definition?

Our answer to both questions is *no*.

First, none of the definitions used in the literature are precise. For example, some authors write that signals are represented by currents in current-mode circuits and by voltages in voltage-mode circuits. This is not a precise definition, because every circuit node has an associated voltage and every branch an associated current, and it is a matter of definition which ones represent signals and which ones do not. It does not seem possible to refine this definition such that it still includes all kinds of signal-processing circuits.

There are no precise and comprehensive definitions in the literature

---

[1]Private communication.

A precise *and* comprehensive definition would be useless

To give a simple example, it is sometimes said that a current mirror is a current-mode circuit, since the currents have a linear relation to the signal, which the voltage over the diode-connected transistor has not. This argument, however, gives problems as soon as it is applied to log-domain filters. Although one could refine the definition again, and again, ad infinitum, doing this is useless because the definition will ultimately become a list that states for every imaginable class of circuits whether it operates in the current mode or the voltage mode, and such a list cannot be used to derive general statements about current-mode and voltage-mode circuits.

The value of an implicit definition

Nevertheless, the current-mode approach to IC design proposed in [Toumazou90] and in many newer papers has clearly had a great impact on IC design. Several new circuits and amplifiers (e.g., the operational floating conveyor discussed in the previous chapter) emerged from this way of thinking. We think that the success of the current-mode idea did not occur *in spite* of the lack of a precise definition, but *because* of the lack of a precise definition. In other words, reading the papers of the current-mode community does not enable the reader to explicitly *define* the current-mode approach, but it does enable him to *apply* it. This is because, from a certain level of complexity on, an implicit definition can convey much more information than any explicit definition possibly could. An implicit definition can, however, not make it possible to clearly fence off current mode from voltage mode.

Making a clear divide would be a disadvantage

Should such a clear divide be made? We think not. The current-mode approach is mainly an alternative way of looking at analogue IC design, and *not* a tool to classify circuits. Taken in this sense, the current-mode idea is a powerful concept mainly because it broadens the horizon of analogue IC design. A clear definition would actually destroy its explanatory power.

Outline of the remainder of this chapter

In Sec. 3.4, we will discuss several recent attempts to show there is a significant performance difference between a current-mode circuit and a voltage-mode circuit, and, in every case, we will give technical reasons for the occurring performance differences that have nothing to do with the signal mode. But first we will present the concepts of circuit transposition in a new way.

Circuit transposition using signal-flow graphs   3.3

Introduction to circuit transposition   3.3.1

A linear circuit Ξ can always be described by two frequency-domain equations,

$$(3.1) \qquad \mathbf{A}\,\mathbf{x} = \mathbf{b}\,U$$

$$(3.2) \qquad Y = \mathbf{c}^{\mathrm{T}}\mathbf{x}$$

where U is the input signal, Y is the output signal, $\mathbf{A}$ is the $(m+n) \times (m+n)$-dimensional matrix that contains the coefficients of a complete set of linearly independent network equations describing Kirchhoff's current law at n different nodes and Kirchhoff's voltage law around m different loops, and $\mathbf{x}$ is an $m+n$-dimensional vector of independent network variables. Vector $\mathbf{b}$ indicates how the input signal is connected to the network, and $\mathbf{c}$ describes how the output signal is derived from the network. Normally, all of them are functions of s, so we omit s for reasons of brevity. The transfer function of Ξ is then

$$(3.3) \qquad T(s) = \frac{Y(s)}{U(s)} = \mathbf{c}^{\mathrm{T}}\mathbf{A}^{-1}\mathbf{b}\,.$$

The operation of replacing $\mathbf{A}$ by $\mathbf{A}^{\mathrm{T}}$ and swapping $\mathbf{b}$ and $\mathbf{c}$ is called *circuit transposition*. The new circuit Ξ_{t} is *dual* to Ξ. It has the transfer function

$$(3.4) \qquad T_{\mathrm{d}} = \frac{Y_d}{U_d} = \mathbf{b}^{\mathrm{T}}\left(\mathbf{A}^{\mathrm{T}}\right)^{-1}\mathbf{c}\,.$$

T_{d} can be interpreted as a 1×1 matrix and can be transposed like any other matrix. Trivially, 1×1 matrices are not changed by transposition:

$$T_{\mathrm{d}} = T_{\mathrm{d}}{}^{\mathrm{T}} = \mathbf{b}^{\mathrm{T}}\left(\mathbf{A}^{\mathrm{T}}\right)^{-1}\mathbf{c} = \left(\mathbf{b}^{\mathrm{T}}\left(\mathbf{A}^{\mathrm{T}}\right)^{-1}\mathbf{c}\right)^{\mathrm{T}}$$

$$(3.5) \qquad = \mathbf{c}^{\mathrm{T}}\left(\left(\mathbf{A}^{\mathrm{T}}\right)^{-1}\right)^{\mathrm{T}}\mathbf{b} = \mathbf{c}^{\mathrm{T}}\mathbf{A}^{-1}\mathbf{b} = T\,.$$

Thus it is established that the transfer function of the dual circuit and the transfer function of the original circuit are identical.

What is circuit transposition really?

Up to here, the discussion was only an exercise in linear algebra, but the most important question has been left unanswered: what does it actually mean for a circuit if $\mathbf{A}$ is replaced by $\mathbf{A}^T$ and $\mathbf{b}$ and $\mathbf{c}$ are exchanged? To answer this question, it is necessary to specify $\mathbf{x}$ more precisely. In the literature, $\mathbf{x}$ typically consists of all node voltages and several branch currents. It can then be shown by matrix algebra how a concrete circuit can be transposed, either directly [Bhattacharyya71] or by way of so-called intermediate transfer functions [Roberts89b, Roberts90]. An alternative way to show how a circuit must be transposed is to start with the more general concept of adjoint circuits [Director69], which also deals with non-linear circuits, and of which linear circuit transposition is just a special case.

Why another proof is necessary

These proofs are un-intuitive for most engineers and engineering students, because abstract network theory is scarcely taught anymore. Today, circuit transposition is often explained by stating that the passive part of the network does not change and by giving transposition tables for the active elements in the circuit (c.f. [Bhattacharyya71, Carlosena92, Carlosena93, Moschytz94]). It is demonstrated in this section how the whole problem can be tackled using signal-flow graphs. This has the advantage that the concept of circuit transposition becomes intuitive for all engineers who have some understanding of signal-flow graphs (SFGs) or feedback block diagrams.

Outline of this section

In the following, we will first introduce the so-called *driving-point signal-flow graphs* (DP SFGs). Then we will define SFG transposition and show how the circuit corresponding to a transposed SFG can be derived. Finally, we will show that transposing the DP SFG of a circuit really is the same as transposing the circuit itself.

3.3.2   Driving-point impedances and signal-flow graphs

Driving-point signal-flow graphs

A new technique to analyse linear networks was presented recently, which combines driving-point impedance analysis

with signal-flow graph (SFG) analysis [Ochoa98]. We will now explain this technique by using an example, but in a different way than it was explained in [Ochoa98].

Fig. 3.1 shows an active-RC low-pass filter, consisting of four passive elements, R_1, R_2, C_1, and C_2, and one active element, a voltage amplifier (or voltage-controlled voltage source, VCVS) with gain α_V. Its nodes are numbered from **1** to **4**. Driving-point analysis, as presented in [Ochoa98], bases on the following simple observation: If a voltage source is connected to node j and its voltage V_j is set such that no current flows through the source, then nothing changes. This condition can also be expressed in terms of V_j: If a voltage source is connected to node j, and if its voltage V_j is set to the node voltage the circuit had before the source was connected, nothing changes. Note that these auxiliary sources are essentially *controlled* sources, since the appropriate V_j depends on the input signal. Nevertheless, the source superposition theorem is still valid for these special controlled voltage sources, since they are chosen explicitly such that they have no influence whatsoever on the circuit. A formal proof of this statement expresses the same idea mathematically to show that the superposition condition [Chen95] still holds; is omitted here for reasons of brevity.

In order to obtain a complete set node voltages and associated branch currents, one current must be assigned to every node voltage. For the nodes with zero node impedance, i.e., the nodes to which a voltage source or a current sink is connected, the current through the voltage source or current sink is chosen. Auxiliary voltage sources are connected to all nodes with non-zero node impedance, e.g., the nodes **2** and **3** in Fig. 3.1.

Fig. 3.2 shows the filter with auxiliary voltage sources connected to the nodes **2** and **3**. Since voltage sources are now present at all nodes, applying the source superposition theorem is a straightforward procedure. For example, the current flowing into the auxiliary source 2 can be expressed as
(3.6)

$$I_{z2} = V_1 \cdot \frac{1}{R_1} - V_2 \cdot \left(\frac{1}{R_1} + \frac{1}{R_2} + sC_1 \right) + V_3 \cdot \frac{1}{R_2} + V_4 \cdot sC_1 \, .$$

By definition of the auxiliary sources, $I_{z2} = 0$. If we denote the sum of currents contributed by all voltage sources but source 2

Introducing auxiliary sources

Where to introduce auxiliary sources

Applying the source superposition theorem to the auxiliary sources
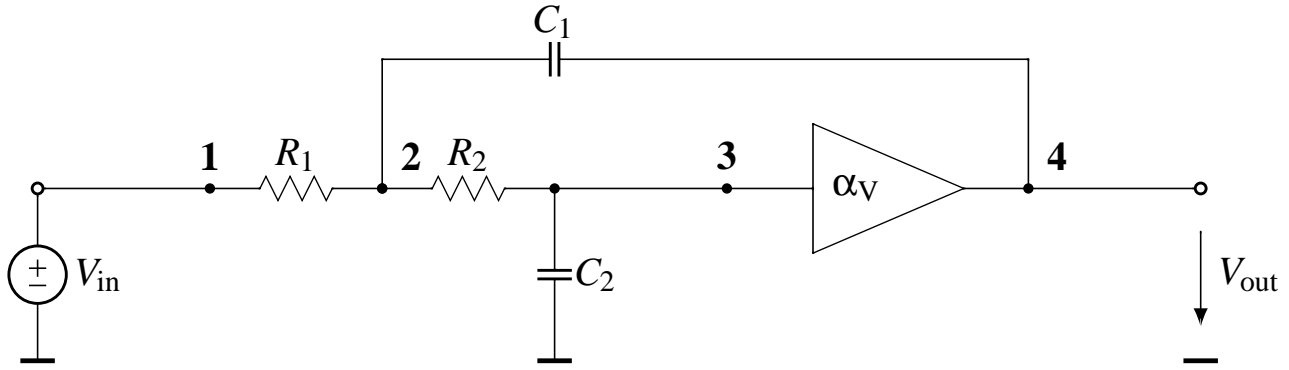
Figure 3.1 *Voltage-mode Sallen-and-Key low-pass filter.*
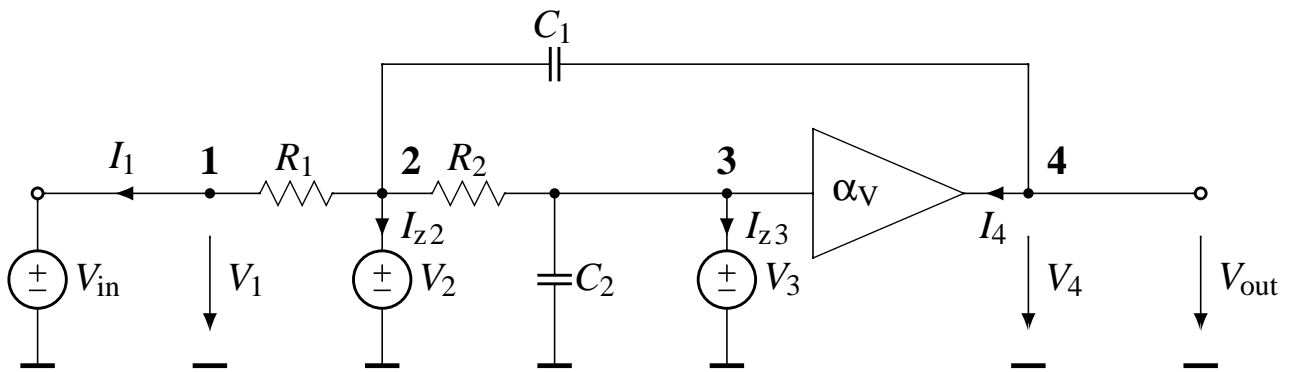
Figure 3.2 *The same filter with auxiliary sources.*
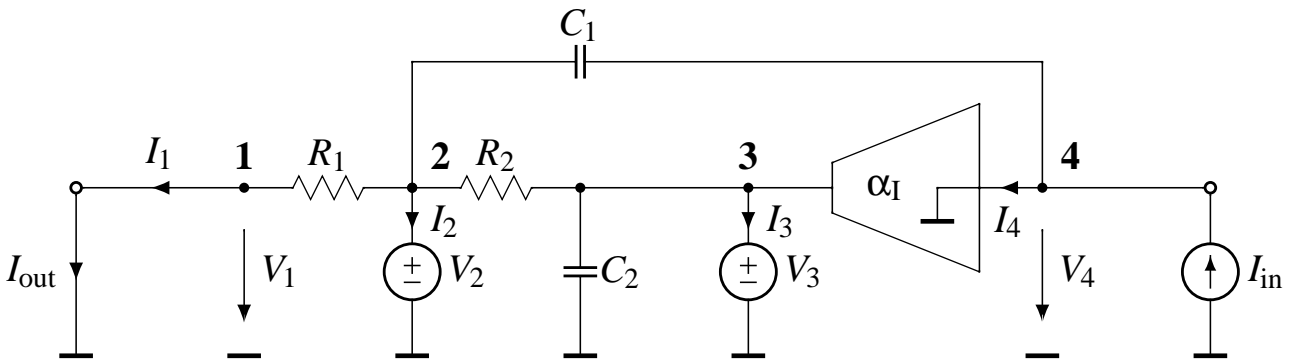
Figure 3.3 *Current-mode filter.*

as I_2, then equation (3.6) can be rewritten as follows:

$$(3.7) \quad V_2 = I_2 \cdot \left(\frac{1}{R_1} + \frac{1}{R_2} + sC_1 \right)^{-1} = I_2 \cdot Z_2$$

$$\text{with} \quad I_2 = V_1 \cdot \frac{1}{R_1} + V_3 \cdot \frac{1}{R_2} + V_4 \cdot sC_1 .$$

Z_2 is called the *driving-point impedance* at node **2** under the condition that all sources but source 2 are set to zero.

Equation (3.7) can directly be drawn in form of a signal-flow graph, shown in Fig. 3.4. It is obvious from the derivation above how the branches "belonging" to the auxiliary source connected to node j are formed:

<div style="float:right">Drawing the driving-point equations as a signal-flow graph</div>

1. There is one branch from I_j to V_j. Its weight is Z_j, the driving-point impedance at node k under the condition that $V_k = 0$ for all $k \neq j$.
2. For each node k, with $k \neq j$, there is a branch from V_k to I_j if and only if the two nodes are directly connected by a component. If this is so, the weight of the branch is the admittance of the connecting component.

This procedure can easily be repeated for the auxiliary source 3, as shown in Fig. 3.5.

It is still necessary to describe the amplifier, and how the input source and the filter output are connected to the circuit:

<div style="float:right">Adding paths describing the active element</div>

$$(3.8) \qquad V_4 = \alpha_V V_3 , \quad V_1 = V_{in} , \quad V_{out} = V_4 .$$

The result is shown in Fig. 3.6. It appears that the variables I_1 and I_4 are not used at all, but it will presently become apparent that it is good from a didactic point of view to include them into the signal-flow graph.

Note that the signal-flow graph in Fig. 3.6 has two loops. It is also possible, using a different technique, to directly derive a signal-flow graph for the filter in Fig. 3.1 which has only one loop [Moschytz94]. Then Mason's gain rule is easier to apply. However, the technique presented here has two great advantages: it can be applied to *any linear circuit* (it is especially easy to apply it to Gm–C filters), and it can be applied *mechanically*. This makes it possible to use it for deriving dual circuits.

<div style="float:right">Advantages and disadvantages of driving-point signal-flow graphs</div>
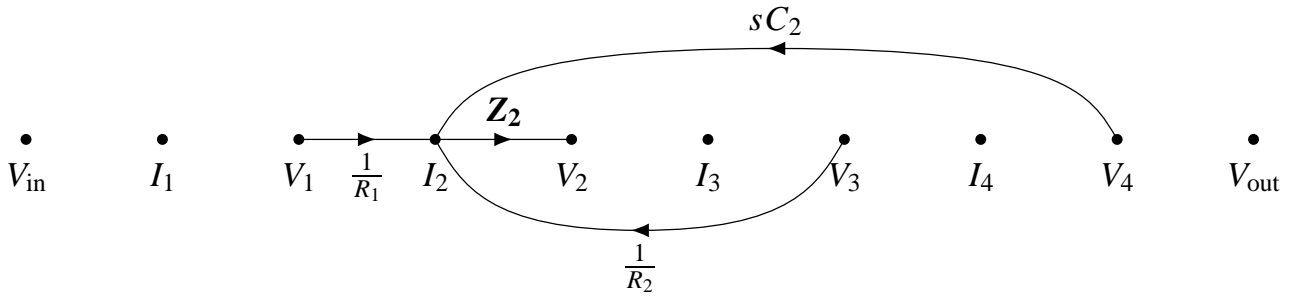
Figure 3.4   *Equation (3.7) drawn as a signal-flow graph.*
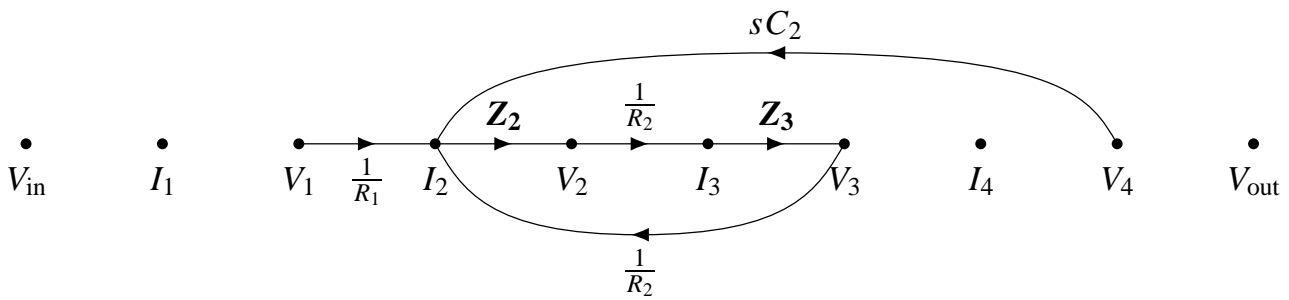
Figure 3.5   *Signal-flow graph branches
                              "belonging" to the two auxiliary sources.*
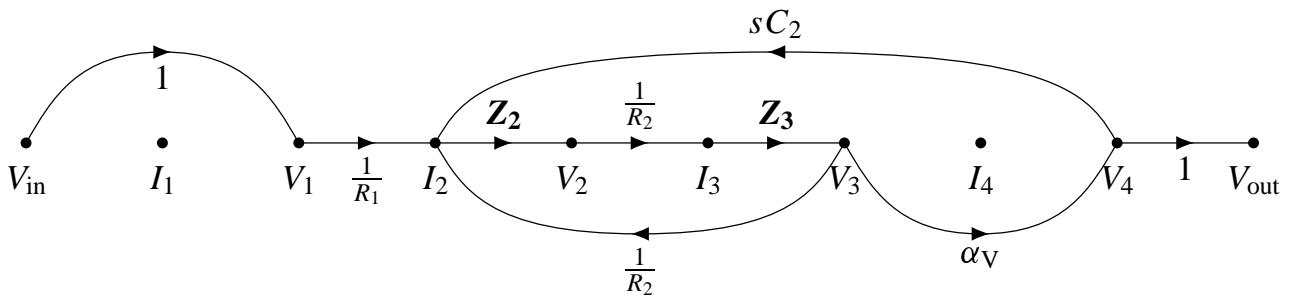
Figure 3.6   *Complete signal-flow graph of the circuit in Fig. 3.2.*
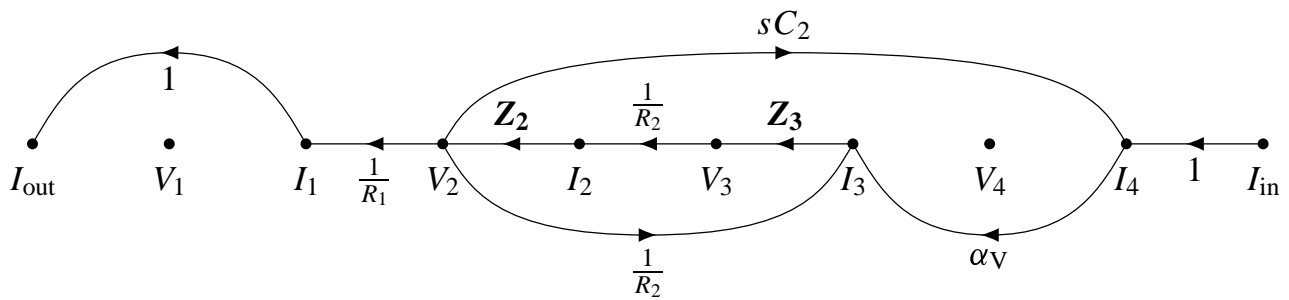
Figure 3.7   *Transposed signal-flow graph describing
                              the circuit in Fig. 3.3.*

Transposition of signal-flow graphs 3.3.3

In this section, all the rules for transposing circuits are derived using only the driving-point signal-flow graph described in the previous section. The only element of signal-flow graph theory required for the proof is Mason's gain rule, which he introduced in [Mason53] and proved in [Mason56], and which can be found in any textbook covering signal-flow graphs. It is, in Mason's notation:

$$(3.9) \qquad G = \frac{\sum_k G_k \Delta_k}{\Delta} \; .$$

Δ is called the graph determinant. It is of the form

$$(3.10) \qquad \Delta = 1 - S_1 + S_2 - S_3 + \dots \; ,$$

where S_1 is the sum of all loops, S_2 is the sum of all products of two loops without common nodes, and S_j is the sum of all products of j loops without common nodes. G_k is the gain of the k-th forward path, and Δ_k is the part of the graph determinant which contains only loops that do not have nodes in common with the path G_k. What G actually is depends on the signal-flow graph in question. For example, the gain of the signal-flow graph in Fig. 3.6 is $G = V_{\text{out}} / V_{\text{in}}$, which is the voltage transfer function T of the circuit in Fig. 3.1.

It can be tedious to evaluate this gain formula for larger circuits, but for our purpose it is enough to note the following: Two graphs have the same gain G if

1. they have the same forward paths,
2. they have the same loops,
3. the topological relations (i.e. common nodes) between the loops and between loops and forward paths are the same.

It now occurs that forward paths and loops as well as the topological relations between them remain unchanged if the direction of all branches of a signal-flow graph are reversed. Therefore the SFG gain also remains the same. We call this operation the *transposition of a signal-flow graph* and the SFG resulting from it the *dual* SFG. For example, this means that the graph in Fig. 3.7 has the same gain as the dual graph in Fig. 3.6. Note that nodes formerly describing voltages

describe currents in the dual graph, and vice-versa. This is necessary since the branch weights are not changed, and, e.g., an admittance branch must still originate from a voltage node and lead into a current node. Therefore $G_d = I_{\text{out}}/I_{\text{in}}$, which means that the circuit corresponding to the dual graph in Fig. 3.7 has the *current* transfer function T. It actually is the dual circuit, which will be shown presently.

Transposition of the circuit example

The passive part remains the same

To find out what the circuit described by the signal-flow graph in Fig. 3.7 looks like, we first note that the new circuit has the same number of nodes. First to the passive branches: The driving-point impedances are still present at the same nodes as before the transposition. The admittance branch from V_j to I_k is now leading from V_k to I_j. Thus the admittances between the nodes do not change either if the circuit is transposed. *The passive part remains the same.*

Inputs, outputs, and amplifiers change

The input voltage source is replaced by a current output, the voltage output by an input current source. Finally, the gain α_V now points from I_4 to I_3: the voltage amplifier is replaced by a current amplifier with a gain of the same absolute value. Note that the current direction *into* the output of a current amplifier (or current-controlled current source, CCCS) is conventionally considered to be positive, but the branch with weight α_V actually contributes a current into the auxiliary source at node **3**, which flows *out* of the current amplifier, which therefore has a gain of $\alpha_I = -\alpha_V$. The resulting circuit is shown in Fig. 3.3.

Derivation of transposition rules

Derivation method

The same method can also be applied to only a part of a circuit, e.g. a single active element: First, the signal-flow graph of the element is drawn, then it is transposed, and finally the active device described by this signal-flow graph is drawn.

Transpose of the differential difference opamp

Take, for example, the differential difference operational amplifier (DDOA) in Fig. 3.8 (c.f. Sec. 2.4). It amplifies the difference of two voltage differences. The transpose derived in Fig. 3.8 is a balanced current opamp with mirrored outputs. Again, since we define positive currents as flowing *into* the output of an active device, but the signal-flow-graph current is
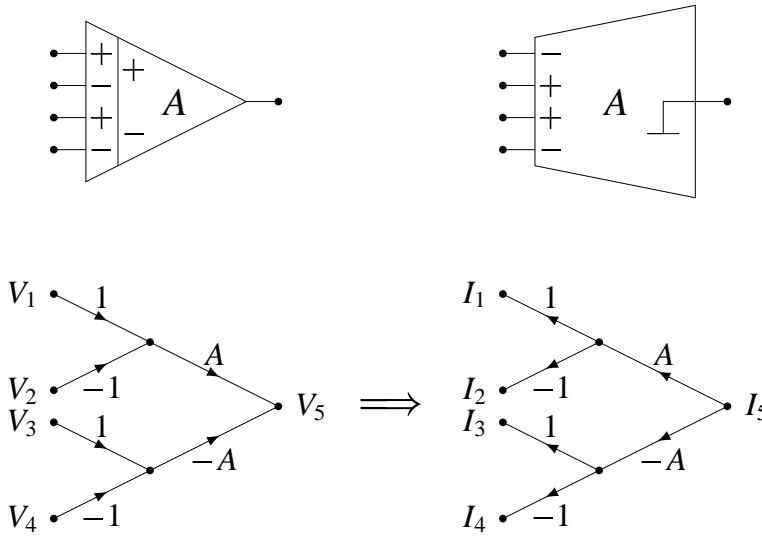
Differential difference opamp. **Figure 3.8**
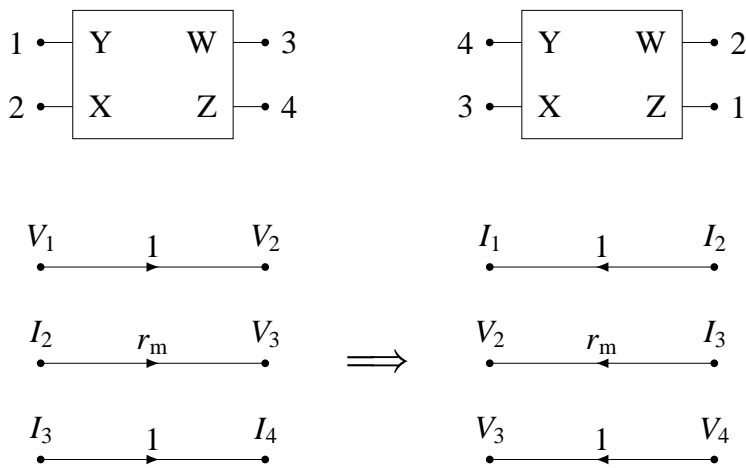
Operational floating conveyor. **Figure 3.9**
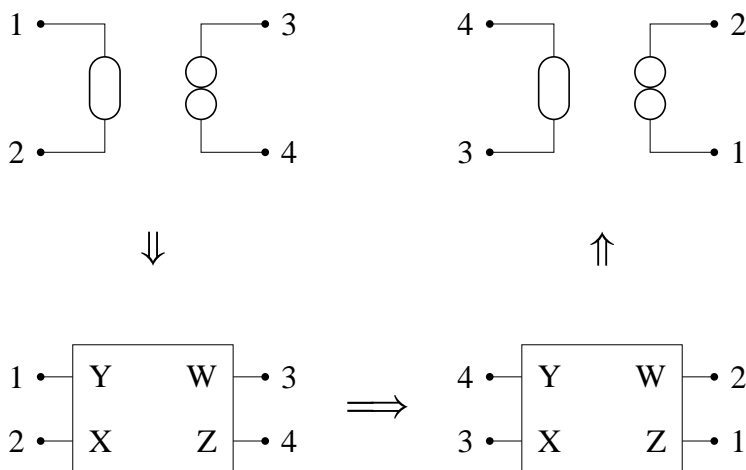
Nullor. **Figure 3.10**

defined as flowing *out of* the output of the passive device, the signs of the current opamp outputs are the inverse of the signs of the DDOA inputs.

Self-dual amplifiers (e.g. OTA, OFC, and CCII−)

A second example is the operational floating conveyor (OFC). As explained in Sec. 2.4, it works as follows: the voltage applied to terminal Y is copied to terminal X. The current flowing into this terminal is then amplified by a very high transresistance r_m, which gives a voltage at terminal W. Finally, the current flowing into terminal W is copied to flow out of terminal Z. From this description, the signal-flow graph of the device follows immediately, but it is important to choose the current directions correctly. The terminals X and W are a current sink and a voltage source, respectively, so I_2 and I_3 are positive if they flow into the OFC. On the other hand, terminals Y and Z are high-impedance terminals, to which either a current sink, a voltage source, or an auxiliary source is connected. In any of these three cases, I_1 and I_4 are positive if they flow out of he OFC. Note that the transpose of this signal-flow graph is identical to the original one. Thus the operational floating conveyor is its own transpose, only the terminals are permuted during transposition, as indicated by the numbers in Fig. 3.9. The same is true for other devices, e.g. the balanced-output OTA and the negative-gain second-generation current conveyor (CCII−), but these proofs are left to the reader.

Transpose of the nullor

One more example: as discussed in Chap. 2, the OFC with $r_m \to \infty$ approximates a four-terminal nullor. Thus the OFC can be used to show that the nullor can be transposed by interchanging nullator and norator, as shown in Fig. 3.10. The same could, of course, also be done by using the balanced-output OTA with $g_m \to \infty$.

3.3.4   SFG transposition and circuit transposition

Systematically writing down SFG equations as matrix equations

We have not yet proved that SFG transposition is the same as circuit transposition. In general, this is not necessarily the case, but it is the case for DP SFGs. The proof is straightforward: the voltages and currents of all nodes occur in the signal vector,

$$(3.11) \qquad \mathbf{x}^\mathrm{T} = \begin{bmatrix} V_1 & V_2 & V_3 & V_4 & I_1 & I_2 & I_3 & I_4 \end{bmatrix}.$$

Then the coefficient matrix can be built by writing down the DP SFG equations in a systematic way: first the equation describing the nodes V_1 to V_4, then the equations describing the nodes I_1 to I_4.

$$(3.12)\quad \mathbf{A} = \begin{bmatrix} y_{1,1} & y_{1,2} & y_{1,3} & y_{1,4} & -1 & a_{1,2} & a_{1,3} & a_{1,4} \\ y_{2,1} & y_{2,2} & y_{2,3} & y_{2,4} & a_{2,1} & -1 & a_{2,3} & a_{2,4} \\ y_{3,1} & y_{3,2} & y_{3,3} & y_{3,4} & a_{3,1} & a_{3,2} & -1 & a_{3,4} \\ y_{4,1} & y_{4,2} & y_{4,3} & y_{4,4} & a_{4,1} & a_{4,2} & a_{4,3} & -1 \\ -1 & b_{1,2} & b_{1,3} & b_{1,4} & Z_1 & z_{1,2} & z_{1,3} & z_{1,4} \\ b_{2,1} & -1 & b_{2,3} & b_{2,4} & z_{2,1} & Z_2 & z_{2,3} & z_{2,4} \\ b_{3,1} & b_{3,2} & -1 & b_{3,4} & z_{3,1} & z_{3,2} & Z_3 & z_{3,4} \\ b_{4,1} & b_{4,2} & b_{4,3} & -1 & z_{4,1} & z_{4,2} & z_{4,3} & Z_4 \end{bmatrix}$$

where $a_{i,j}$ is the weight of the SFG branch going from V_j to V_i, $b_{i,j}$ is the weight of the SFG branch going from I_j to I_i, $y_{i,j}$ is the weight of the SFG branch going from V_j to I_i, and $z_{i,j}$ is the weight of the SFG branch going from I_j to V_i. Note that $z_{i,i}$ is just the driving-point impedance Z_i.

It now becomes apparent what transposing $\mathbf{A}$ means for the DP SFG: any branch that left V_i now enters I_i, any branch that entered V_i now leaves I_i, and so on. This is precisely how the transposition of a signal-flow graph is defined. The effect of interchanging $\mathbf{b}$ and $\mathbf{c}$ on the DP SFG can be investigated in a similar way and thus confirms that SFG transposition is in fact the same as circuit transposition.

Proof of the equivalence

Detailed comparisons   3.4

Ceteris paribus comparisons   3.4.1

To find out whether it makes a difference to represent signals by currents instead of voltages, a *ceteris paribus* (other things being equal) comparison must be made. To our knowledge, only one attempt do do this was published at all [Mahattanakul98]. There the authors compared the two filters shown in Fig. 3.11, which are *not* dual according to the discussion above, but have the same loop structure and the same low-pass transfer

Comparison by figure of merit
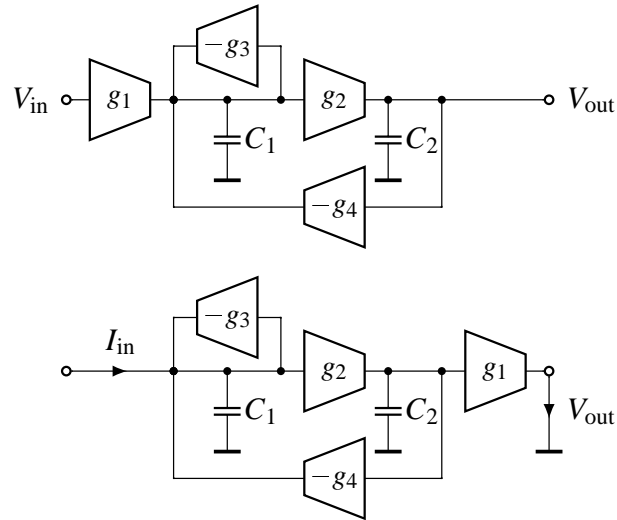
Figure 3.11   *Voltage-mode and current-mode Gm–C filter [Mahattanakul98].*

function.[2] The study takes into account the noise of the OTAs and the soft harmonic distortion induced by their non-linear transconductances, but not clipping effects caused by output stage saturation. It is shown that both circuits have similar amounts of harmonic distortion. The circuits are compared according to a figure of merit,

$$(3.13) \qquad\qquad F = \frac{\mathrm{DR} \cdot f_{\mathrm{p}}^2}{P^2}$$

where DR is the dynamic range, f_{p} is the pole frequency, and P is the power consumption. The result shows that the dynamic range of the voltage-mode filter is better by at most 6 dB in the relevant range of pole Qs and DC gains of the low-pass filter function.

Reason for the perceived performance difference

The problem with this study is that it is not really *ceteris paribus*. The difference mainly occurs because the noise of the input OTA in the voltage-mode filter is processed by the filter, which is not the case for the noise of the output OTA in the current-mode filter. Obviously, if both the input OTA of the voltage-mode filter and the output OTA of the current-mode

---

[2]Actually the filter in Fig. 3.11 realizes two transfer functions. Choosing the node to which C_1 is connected as the output node (top) or input node (bottom) results in a bandpass transfer function, but all that is said in this section applies to the bandpass filters as well.

filter were ideal and noiseless, both filters would perform identically. On a real IC, the voltage-mode circuit needs an output buffer, since a resistive load connected to the output node would otherwise change the transfer function, and the current-mode circuit needs an input buffer, since the input nodes must be driven by a high-resistance device. However, this time the noise of the current buffer is filtered, but not the noise of the voltage buffer, and the performance difference between the two is reduced to the performance difference between the circuits used to insert signals into the feedback loop and extract signals from it. The resulting performance difference is certainly small, and it is not a question of signal representation, but of transistor-level design. Thus, [Mahattanakul98] establishes that, other things being equal, there is no performance difference between the current-mode and the voltage-mode Gm-C filter discussed in the paper.

Feedback amplifiers and open-loop amplifiers 3.4.2

In most of the papers proposing very fast current-mode circuits, open-loop current amplifiers are compared to results obtained with closed-loop voltage amplifiers [Carlosena92, Roberts92, Roberts89a, Wilson92]. Many of the amplifiers derived with a current-mode approach base on current mirrors and provide a specific, low gain without feedback around the amplifier. The typical low-gain voltage amplifier uses feedback around a high-gain amplifier. This feedback stabilises the gain and reduces harmonic distortion, it also improves the terminal impedances of the amplifier.

Feedback around a high-gain amplifier

Fig. 3.12 shows the transfer functions and terminal impedances of the CCII+ in Fig. 2.10 [Schmid98c] and Analog Device's SSM 2135 audio opamp connected as a buffer and in an open-loop configuration. The frequency of the opamp has been scaled by 50 to make the curves comparable. A look at the transfer functions shows that the closed-loop transfer function of the opamp and the open-loop current transfer function of the CCII+ look very similar. The reason is that both transfer functions are determined by non-dominant poles only, the dominant pole of the voltage opamp, whose effect

Qualitative comparison of an opamp and a CCII+
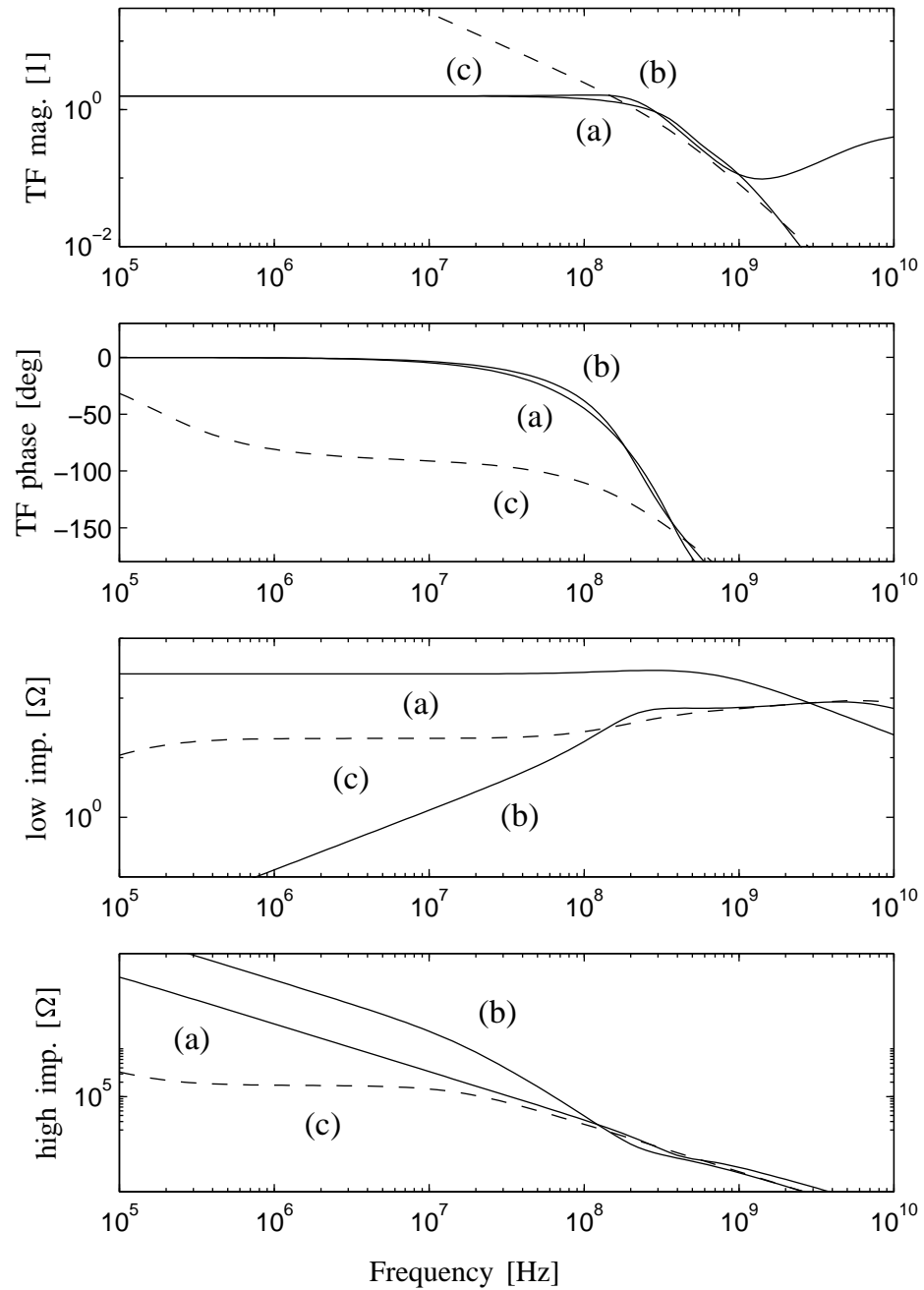
Figure 3.12   *Transfer functions and terminal impedances of (a) the CCII+ in Fig. 2.10, the AD SSM 2135 opamp (b) connected as a voltage buffer and (c) open-loop. The AD SSM 2135 is actually an audio opamp, its frequency has been scaled by a factor of 50 to make the curves comparable.*

is clearly visible in the open-loop transfer function, only plays a stabilising role once the feedback loop is closed (see below). The impedance curves show that feedback decreases the output impedance of the opamp but increases the input impedance, which can be considered an improvement in both cases. However, close to the unity-gain frequency f_1 of the opamp, there is some peaking, which means that feedback actually makes the impedances worse above approximately $f_1/5$. Note that the output impedance of the opamp is far below the input impedance of the CCII+ because the former is built in a bipolar technology, but the latter in CMOS. Although Fig. 3.12 only shows two specific devices, the effects discussed are the same for other amplifiers.

Coming back to gain stabilisation, the low-gain amplifiers used in Sallen-and-Key filters (c.f. Chapter 4) is normally built using one voltage opamp and two resistors, as in Fig. 3.13. Its transfer function is then

Transfer function of an opamp with resistive feedback

$$(3.14) \qquad T(s) = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{A(s)}{1 + \frac{R_1}{R_1 + R_2} A(s)} \, .$$

For very high gains,

$$(3.15) \qquad \lim_{A(s) \to \infty} T(s) = 1 + \frac{R_2}{R_1} = \alpha_{\text{V}} \, ,$$

and if the gain of the amplifier is expressed by the gain-bandwidth product, $A(s) \approx \omega_{\text{gbw}}/s$,

$$(3.16) \qquad T(s) = \frac{\alpha_{\text{V}} \, \omega_{\text{gbw}}}{\alpha_{\text{V}} \, s + \omega_{\text{gbw}}} \, .$$

Calculating the sensitivity of the transfer function to variations in the gain-bandwidth product gives:

Influence of open-loop gain and feedback gain on closed-loop gain stability

$$(3.17) \qquad S_{\omega_{\text{gbw}}}^{T(s)} = \frac{\alpha_{\text{V}} \, s}{\alpha_{\text{V}} \, s + \omega_{\text{gbw}}} \, .$$

Similarly,

$$(3.18) \qquad S_{\alpha_{\text{V}}}^{T(s)} = \frac{\omega_{\text{gbw}}}{\alpha_{\text{V}} \, s + \omega_{\text{gbw}}} \, .$$
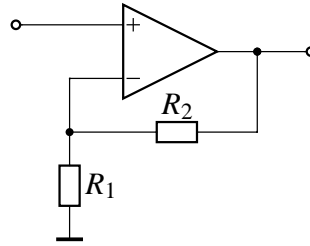
Figure 3.13   *Low-gain voltage amplifier.*

For low frequencies, $S^{T(s)}_{\omega_{gbw}} \approx \frac{\alpha_V s}{\omega_{gbw}}$ and is very small. This means that variations of ω_{gbw} have little influence on the overall gain. On the other hand, $S^{T(s)}_{\alpha_V} \approx 1$ for low frequencies, which means that any variations of the feedback gain directly translates into variations of the overall gain. Thus the overall gain is set by the precision of the ratio of the feedback resistors, which can be very precise on chip. Note that the latter sensitivity can only get smaller for high frequencies, while the sensitivity to variations of the gain-bandwidth product goes towards one for high frequencies. This means that the stabilising effect of feedback around a high-gain amplifier decreases with increasing frequencies. We can now find out at which frequency the contributions to the standard deviation of $T(s)$ caused by the standard deviations of α_V and of ω_{gbw} become equal:

$$(3.19) \quad \overline{\sigma}_{\alpha_V}\, S^{T(s)}_{\alpha_V} = \overline{\sigma}_{\omega_{gbw}}\, S^{T(s)}_{\omega_{gbw}} \quad \Longrightarrow \quad s = \omega_{gbw}\, \frac{\overline{\sigma}_{\alpha_V}}{\alpha_V\, \overline{\sigma}_{\omega_{gbw}}}\ .$$

Feedback amplifiers are better than open-loop amplifiers only at lower frequencies

On CMOS ICs, resistor ratios can be precise to within 0.1 %, while the precision of ω_{gbw} can be around 1 %. Thus, setting e.g. $\alpha_V = 2$, the variance of the ω_{gbw} determines the variance of α_V for frequencies above $\omega_{gbw}/20$, i.e., it normally dominates close to the pole frequency of a Sallen-and-Key filter built with a feedback amplifier. Ideally, the gain variation is then 1 % around the unity-gain frequency of the opamp and decreases with 20 dB per decade towards lower frequencies, but as with the resistances, some over-peaking occurs in practical cases. The feedback opamp can now be compared to CCIIs, whose current gains can also be precise to within 1 %. It then turns out that again, the feedback opamp is decidedly better than the CCII+ only for frequencies below $\omega_{gbw}/5$.

Thus we can now explain why current-mode circuits are considered to be faster than voltage-mode circuits: although both would be similarly good from an ideal point of view, over-peaking caused by second-order effects makes problems close to the ω_{gbw} product of the feedback opamps. It is important to see that the same over-peaking effects also occur in CCIIs that use local feedback to reduce the input resistance of the X terminal; in this case, the speed advantage of the CCII vanishes. It is also possible to build the circuit that is dual to the one in Fig. 3.13 using a current-mode opamp; its performance will then be similar. Furthermore, one can also build open-loop voltage amplifiers that show no over-peaking. However, it turns out that circuits without local stabilising feedback are just *more typical* for the current-mode approach.

Implications on the current-mode vs. voltage-mode debate

Both the transfer function of the closed-loop opamp and the behaviour of the CCII are determined by the low-impedance nodes of the circuits only. These low-impedance nodes all look similar in both voltage-mode and current-mode circuits: a transistor g_{m} sets the node resistance, parasitic capacitances of transistors set the node capacitance, and the voltage swing is limited by transistors that would otherwise leave the region of saturation. Thus the non-dominant poles and zeros will be at similar frequencies, and the harmonic distortion at high frequencies and the noise properties will also be similar. What mainly determines the performance of a circuit is the number of low-impedance nodes and the way they are connected, i.e., the *complexity of a circuit* determines the performance of an amplifier or filter. As with feedback, one finds that less complex circuits are *more typical* for the current-mode approach. There are a few voltage-mode circuits with reduced complexity, like the very fast Gm–C filters presented in [Nauta92] built with OTAs that only have input and output nodes, but no internal nodes at all. Of course, current-mode circuits can also be made more complex to improve their linearity and signal-to-noise ratio, but that slows them down again.

Why current-mode and voltage-mode are not different

Thus the advantages of current-mode circuits that are often cited in the literature, like a potential for reaching higher frequencies, lower power consumption, and smaller chip area, are in fact real, but the reason is not technical, and has nothing to do with choosing voltages or currents to represent

Non-technical reasons for advantages

signals. The reasons for the difference are mainly the design preferences of the proponents of the current-mode approach.

3.4.3   Mixed-signal circuits

Advantages are open to debate

It has been pointed out that using mixed feedback (i.e. voltage to current or current to voltage) may result in speed advantages [Wilson92]. This is also open to debate. We will give two brief examples to illustrate the complexity of such comparisons:

Gm–C filters

Design advantage of Gm–C filters

Gm–C filters can reach higher frequencies than single-amplifier biquads (SABs), but they then also consume more power. From an overview of recently published Gm–C filters, it seems that it is easier to trade speed for power with Gm–C filters than with SABs (c.f. Chap. 8). However, there is still no fundamental reason for Gm–C filters to be faster than single-amplifier filters.

The current-feedback opamp

...has advantages and disadvantages ...

This device, which we already described in Chapter 2, was extensively discussed at the ISCAS 1993 [Bruun93, Bowers93, Franco93, Harvey93, Toumazou93]. The alleged advantages of the CFB opamp are that its bandwidth is very high and independent of the closed-loop gain, that it has no theoretical slew-rate limitation, and that its input-referred noise voltage is low compared to that of opamps. There are several applications in which the CFB opamp performs very well (c.f. Sec. 7.2). Its disadvantages are its inferior DC performance, the asymmetry of its inputs, the high input bias current necessary on the inverting input, and the dependence of its bandwidth on the feedback resistor [Bowers93]. Furthermore, the feedback cannot be capacitive, this would lead to stability problems [Franco93].

...but is not fundamentally better

There is always a trade-off between DC performance and bandwidth in opamps, and CFB opamps seem to be faster mainly because they are compared to voltage opamps having much better DC performance. Then, while the closed-loop gain is independent of the bandwidth, it is limited by the input resistance of the current-input terminal. Especially when the CFB opamp is set to its maximum bandwidth, the available

range of gain is surprisingly small. Furthermore, CFB opamps draw a considerable supply current under slewing conditions; thus, although the slew rate of the CFB opamp is indeed very high, it is set by the supply in practical applications. Many other problems were described in [Bowers93, Harvey93, Franco93].

Conclusion   3.5

The notion of looking at circuits in terms of node impedances made it possible to derive a new, constructive proof of the circuit transposition theorem using signal-flow graphs. A discussion based on the same notion showed that there is no fundamental difference between current-mode and voltage-mode circuits. While it is true that many current-mode circuits live up to the reputed advantages of the current mode, the reason is not that current has been used as a signal, but that circuit simplicity, lower power consumption and speed are often achieved at the cost of higher distortion, higher gain variation, and so on.

The mode is not decisive

What would happen if a designer set out to build a current-mode opamp that has approximately the same properties (CMRR, PSRR, linearity, chip area, etc.) as, e.g, the well-known opamp LM 741, but with the maximum possible speed? In the light of the above discussion, we believe that the speed would also be approximately the same, but until somebody tries this, which is not likely because the effort would be immense, the question will remain open.

On the difficulty of a valid comparison

Chapter 4

Single-amplifier biquadratic filters (SABs)

**The opposite of a correct statement
is a false statement.
But the opposite of a profound truth
may well be another profound truth.**

(Niels Bohr)

This chapter introduces the concepts behind single-amplifier biquadratic filters and then discusses the sensitivity of the pole Q to component variations and the influence of amplifier non-idealities on the transfer function.

In Sec. 4.3, it is shown using sensitivity theory that a Sallen-and-Key low-pass filter with minimum pole-Q variance always has a gain less than two. The formulae derived in Sec. 4.4 can be used both in the design cycle to do pre-distortion of component values and more generally to determine the maximum pole frequency that can be achieved with a given amplifier.

Both sections are original work, but while the results of Sec. 4.4 might also be found scattered over the literature, several results presented in Sec. 4.3 are new, and some even contradict textbook knowledge.

4.1   Background

I had already heard a lot about SABs during my studies, and I always found the exercises easy enough to solve. However, when I tried to design my first SAB, I found out that I did not actually know how to treat amplifier non-idealities, and I could not find much about this in textbooks either. The reason is that in the times when the theory of SABs was developed, one did not try to push the pole frequency of the SABs to the extreme, so amplifier non-idealities were not so important back then. Thus I had to write down that theory for myself, and presented it as a paper at the ISCAS 98 [Schmid98c]. It is now Sec. 4.4 of this thesis.

Next I tried to calculate and optimise the sensitivity of the pole Q to component variations. I saw that the approximations that are usually made in order to apply sensitivity theory were not necessarily valid for filters using open-loop amplifiers, so I tried to find an exact expression in the literature and was very surprised that there was none to be found. I realised why this was so when I first wrote down the exact expression for the variance of the pole Q of a Sallen-and-Key low-pass filter and saw its complexity.

The main reason why I could solve this expression that was not solved before is that I used modern data visualisation tools and played with numerical examples of the function to be optimised. Once I had noticed the symmetry I exploit in Sec. 4.3, solving the optimisation problem became comparatively easy.

4.2   Introduction to SABs

4.2.1   Classification of SABs

Origin

The single-amplifier biquadratic filters were first put in a common framework in 1980 [Moschytz80]. As an introduction
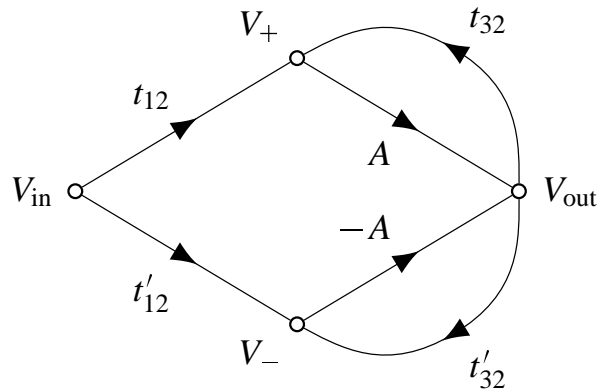
General signal-flow graph of a single-opamp biquad. **Figure 4.1**

to SABs, we explain the classification from [Moschytz80] briefly, using our own concepts.

Moschytz's classification covers all SABs that are built with one opamp and an RC network, have one voltage input, and use the opamp output as the filter output. Such filters can generally be drawn by the signal-flow graph (SFG) in Fig. 4.1 that has only four nodes: the input and output voltage of the filter, V_{in} and V_{out}, and the two opamp input voltages, V_+ and V_-.

Classifying opamp-RC SABs

The SABs that can be described by this SFG can also be classified using four criteria:

Four classification criteria

1. The number of forward paths, which can be one (Type I) or two (Type II).
2. The number of feedback paths, which can be one (single feedback, SF) or two (double feedback, DF). In the latter case, either t_{32} or t'_{32} is normally constant over the s plane (i.e., it contains only resistors), because using two frequency-dependent feedback paths does not give more functionality.
3. The filter function of the frequency-dependent feedback path, which can be a low-pass (class 1), high-pass (class 2), band-reject (class 3) or band-pass filter (class 4).
4. The filter function of the complete filter.

For example, the SAB shown in Fig. 4.3 on p. 67 is a I–SF–4–LP filter.

All SABs generate complex poles by forming the difference of two rational fractions that have only real poles. For I–SF

Generation of complex poles
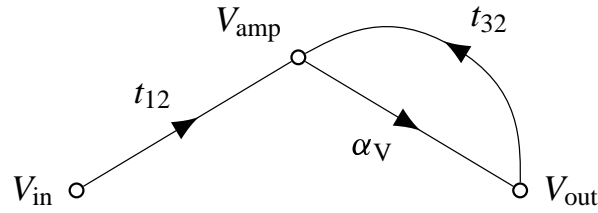
Figure 4.2   *Signal-flow graph of a I–SF filter.*

filters, the SFG in Fig. 4.1 can be simplified. Using an arbitrary
voltage gain α_V results in the SFG shown in Fig. 4.2. If t_{12} and
t_{32} are both produced by the same RC network, they will only
have different numerators, the denominator is the same:

$$(4.1) \qquad t_{12} = \frac{n_{12}}{\hat{d}}, \quad t_{32} = \frac{n_{32}}{\hat{d}},$$

where the hat on $\hat{d}$ indicates a second-order polynomial that
has two negative, real roots. It follows from the SFG that the
transfer function of the I–SF filter is

$$(4.2) \qquad T(s) = \frac{V_{out}}{V_{in}} = \frac{\alpha_V\, t_{12}}{1 - \alpha_V\, t_{32}} = \frac{\alpha_V\, n_{12}}{\hat{d} - \alpha_V\, n_{32}}.$$

The new denominator can be written as

$$\hat{d} - \alpha_V\, n_{32} = (a_2 - \alpha_V\, b_2)\, s^2 + (a_1 - \alpha_V\, b_1)\, s + (a_0 - \alpha_V\, b_0)$$
$$(4.3) \qquad = c_2\, s^2 + c_1\, s + c_0 .$$

The roots of this expression are

$$(4.4) \qquad s_{1,2} = -\frac{c_1}{2\, c_2} \pm \frac{\sqrt{c_1^2 - 4\, c_2\, c_0}}{2\, c_2},$$

and the pole frequency, the pole quality factor and the 3-dB
bandwidth become

$$(4.5) \qquad \omega_p^2 = \frac{c_0}{c_2}, \quad q_p = \frac{\sqrt{c_0\, c_2}}{c_1}, \quad \omega_{3\,dB} = \frac{c_1}{c_2}.$$

The poles of such filters become complex if the second term in
(4.4) becomes imaginary, i.e., if $c_1^2 - 4\, c_2\, c_0 < 0$. This can be
achieved in three different ways by making $c_2\, c_0$ larger, or by
making c_1 smaller.

	n_{32}	feedback	α_V	
1	c_0	low-pass	–	constant bandwidth
2	$c_2 s^2$	high-pass	–	low ω_p possible
3	$c_2 s^2 + c_0$	band-reject	–	constant ω_p
4	$c_1 s$	band-pass	+	constant ω_p

Four classes of SABs   **Table 4.1**

These four possibilities define the four filter classes which are shown in Table 4.1. As follows directly from the equations above, the bandwidth of class-1 filters does not change when α_V is adjusted, class-2 filters can reach very low frequencies because an increase of α_V reduces ω_p, and filters of the classes 3 and 4 have an ω_p that is independent of α_V.

Four filter classes

The disadvantage of the classes 1 and 2 is that they do not contain high-pass and low-pass filters, respectively. The problem with class-3 filters is that $n_{32} = c_2 s^2 + c_0$ can only be realised with a third-order RC network, a second-order RC-network gives an $n_{32} = c_2 s^2 + c_1 s + c_0$ with a $c_1 > c_{1\min} > 0$ that limits the maximum achievable pole quality factor to $q_p < \infty$ (this is a way of expressing the Fialkow-Gerst condition, c.f. [Moschytz80]).

Restrictions of classes 1–3

The most versatile class is therefore class 4, or the class of Sallen-and-Key filters, named after R. P. Sallen and E. L. Key, who described several filters of this class in [Sallen55]. The whole classification can easily be applied to current-opamp filters as well (through circuit transposition, c.f. Sec. 3.3 or [Moschytz94]). It is also applicable to SABs built with different amplifiers, since most of them have only one frequency-dependent feedback path whose filter function can easily be determined.

Class 4 is the most versatile class

Some properties of Sallen-and-Key filters   4.2.2

The main advantage of Sallen-and-Key filters is that they can produce a high q_p even with a low gain α_V, as was already mentioned in Sec. 3.4.2. The main disadvantage is that the q_p of Sallen-and-Key filters is more sensitive to variations of component values than it is in some multiple-amplifier biquads.

High q_p sensitivity

Only low gain
necessary

We will show in Sec. 4.3 that, for low-pass filters, the gain α_V need never be greater than 2 to minimise the variance of q_p. This explains why Sallen-and-Key filters are sometimes called "low-gain active filters" [Allen95].

Amplifier
non-idealities

The ω_p and q_p as well as the stopband attenuation of a Sallen-and-Key filter depend on the amplifier non-idealities like input impedance, output impedance, and phase lag. The effects of these non-idealities are discussed in Sec. 4.4, and it is shown that the phase lag of the amplifier increases q_p as in Gm–C filters, and that a non-ideal low-impedance terminal introduces a parasitic zero that limits the obtainable stopband attenuation and with that also the maximum achievable ω_p.

4.3   Sensitivity

4.3.1   Introduction

Approximation before
optimisation?

One of the disadvantages of SABs is the comparatively high sensitivity of the pole quality factor q_p to variations of the passive component values and of the amplifier gain. Design equations for minimising the variance of q_p are well known (cf. [Huelsman80, Moschytz81]), but they were all derived by first making approximations and then solving for a minimum-variance filter.

Optimising without
approximations

In this section, we solve the optimisation problem without making any approximations other than applying sensitivity theory. We first derive closed-form design equations for the Sallen-and-Key low-pass filter using a non-linear coordinate transform. We then prove some general properties of the minimum-sensitivity filter: First, the values of its passive components are spread as far as possible; second, the capacitor spread is larger than the resistor spread; and last, but not least, the gain of the minimum-sensitivity filter must be less than two.

Unity-gain filters

A similar discussion for the unity-gain low-pass filter provides an even more interesting result: if the pole frequency is below a certain limit determined by the amplifier, the variance of the resistors, and q_p, then the minimum-sensitivity filter has *very*
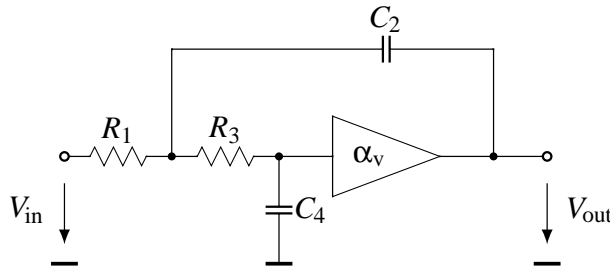
Biquadratic Sallen-and-Key low-pass filter.   **Figure 4.3**

low component spreads. Although this will not happen for high-Q filters with a pole frequency pushed to the physical limits, many low-Q anti-aliasing filters are better built with very low component spreads, a result that contradicts well established beliefs but is confirmed by Monte-Carlo simulations.

The whole derivation is made for discrete-component voltage-mode filters. Obviously, it is valid as well for current-mode filters. In the end, we show that there is only a quantitative difference between discrete-component and integrated filters, thus establishing that the gain of a minimum-sensitivity filter is always below two in both cases.

Discrete-component and integrated filters

Arbitrary-gain Sallen-and-Key low-pass filter

4.3.2

Figure 4.3 shows a second-order Sallen-and-Key low-pass filter. To simplify the arithmetic, its passive components can be written as $R_1 = R/n$, $R_3 = R \cdot n$, $C_2 = C/m$ and $C_4 = C \cdot m$. Then R and C are the geometric means of R_1, R_3 and C_2, C_4, n and m are the *component-spread factors* of the resistors and the capacitors, and the component spreads are $\max\{n^2, 1/n^2\}$ and $\max\{m^2, 1/m^2\}$. The transfer function of the filter is then

Make ω_p and q_p orthogonal to calculate sensitivities

$$(4.6) \qquad T(s) = \alpha_V \frac{\omega_p^2}{s^2 + \frac{\omega_p}{q_p} s + \omega_p^2} \,,$$

$$\text{with} \quad \omega_p = \frac{1}{RC} \,, \quad \frac{1}{q_p} = mn + \frac{m}{n} + \frac{1 - \alpha_V}{mn} \,,$$

where ω_p is the pole frequency in rad/s and q_p is the pole quality factor. ω_p and q_p have the following sensitivities to

variations of the active and passive components:

(4.7a) $S_{\alpha_V}^{\omega_p} = 0, \quad S_{\alpha_V}^{q_p} = \alpha_V/D, \quad S_{R_{1,3},C_{2,4}}^{\omega_p} = -1/2,$

(4.7b) $S_{R_1}^{q_p} = -S_{R_3}^{q_p} = \left(m^2 n^2 - m^2 - 1 + \alpha_V\right)/2D,$

(4.7c) $S_{C_2}^{q_p} = -S_{C_4}^{q_p} = \left(m^2 n^2 + m^2 - 1 + \alpha_V\right)/2D,$

where $D = m^2 n^2 + m^2 + 1 - \alpha_V.$

<div style="float:left; width:30%;">

Choose a practically relevant optimisation criterion

</div>

It becomes apparent from (4.7a)–(4.7c) that, using resistors and capacitors of a given precision, only the sensitivities of q_p differ for different designs. Therefore, all that can be done is to minimise the variance of q_p in function of the variances of the component values. The expressions become simpler if *relative* variances are used, e.g. $\overline{\sigma}_{R_1}^2 = \sigma_{R_1}^2/R_1^2$. Then

(4.8) $\overline{\sigma}_{q_p}^2 \approx \sum_{x \in X} \left(S_x^{q_p}\right)^2 \overline{\sigma}_x^2, \quad X = \{R_1, C_2, R_3, C_4, \alpha_V\},$

which is a generalised variant of *Schoeffler's multivariate criterion*. Substituting (4.7a)–(4.7c) into this equation results in a closed-form expression for $\overline{\sigma}_{q_p}^2$. Finding all local minima now means setting the gradient to zero, i.e. solving the vector equation $\nabla \overline{\sigma}_{q_p}^2 = \mathbf{0}$ for m and n, which cannot be done directly.

<div style="float:left; width:30%;">

Separate $\nabla \overline{\sigma}_{q_p}^2 = \mathbf{0}$ by a non-linear coordinate transform

</div>

Visualising numerical examples of the functions (4.8) around $m = n = 1$ shows, however, that they all have a form similar to the one shown in Fig. 4.4. A "valley" towards the right is apparent, which can be brought into the direction of an axis using a simple non-linear coordinate transformation,

(4.9) $x = mn, \quad y = \dfrac{n}{m}, \quad$ with $m, n, x, y > 0,$

which is just a 45-degree rotation of the logarithmic coordinate system. The new coordinates are shown as white lines in Figure 4.4.
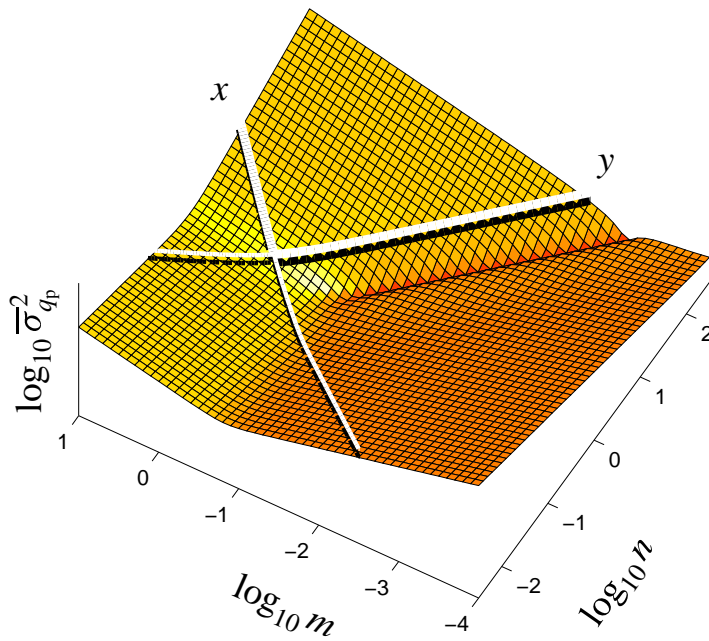
Example of $\overline{\sigma}_{q_p}^2$ with the x, y coordinate system shown by white lines.

Figure 4.4
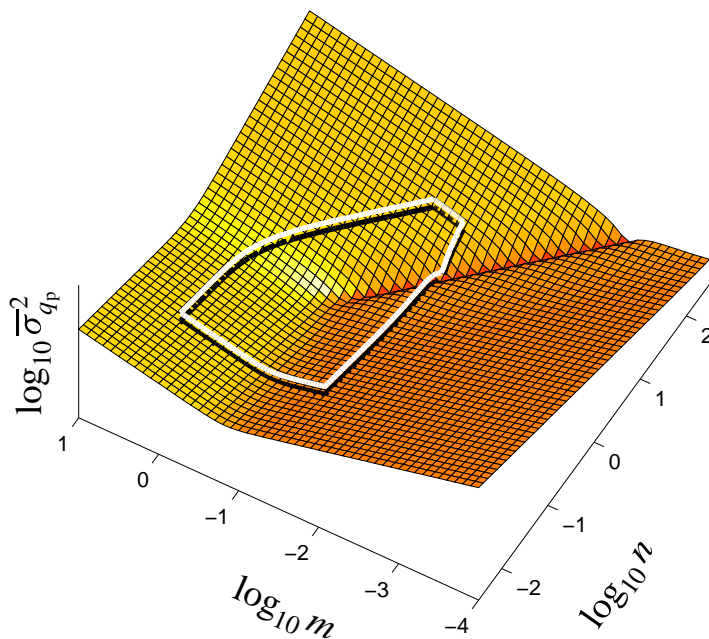
Surface from Fig. 4.4 with the boundary described by $\alpha_V < 5$, component spread < 1000.

Figure 4.5
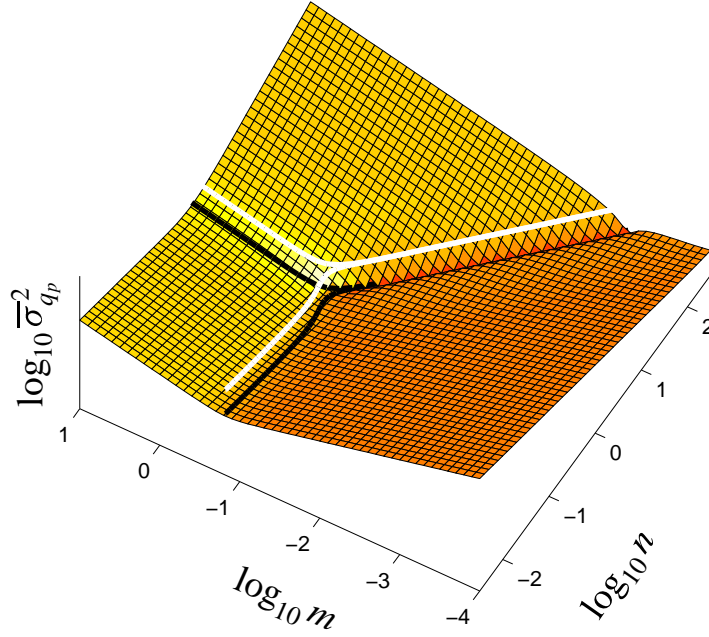
Figure 4.6   *Example of $\overline{\sigma}^2_{q_p}$ showing white lines above the surface where $\nabla_m \overline{\sigma}^2_{q_p} = 0$ and $\nabla_n \overline{\sigma}^2_{q_p} = 0$.*

Design equations

Solving $\nabla \overline{\sigma}^2_{q_p} = \mathbf{0}$ in the new coordinates is an almost trivial task. We give the results in implicit form; the explicit form exists but is too complicated to provide insight.

$$0 = 2q_p\overline{\sigma}^2_R(2\overline{\sigma}^2_C + \overline{\sigma}^2_{\alpha_v})x^4 - \overline{\sigma}^2_R(2\overline{\sigma}^2_C + \overline{\sigma}^2_{\alpha_v})x^3$$

(4.10a)
$$+ \overline{\sigma}^2_C\overline{\sigma}^2_{\alpha_v}x - 2\overline{\sigma}^2_C\overline{\sigma}^2_{\alpha_v}q_p \,,$$

(4.10b) $$y = \frac{-q_p x(2\overline{\sigma}^2_C + \overline{\sigma}^2_{\alpha_v})}{q_p(2\overline{\sigma}^2_C + \overline{\sigma}^2_{\alpha_v})x^2 - (\overline{\sigma}^2_C + \overline{\sigma}^2_{\alpha_v})x + \overline{\sigma}^2_{\alpha_v}q_p} \,.$$

No local optimum

We show in the appendix on p. 75 that this system of equations has no solution for $q_p > \frac{1}{2}$ with $x, y > 0$. Thus the minimum-sensitivity solution lies on the boundary defined by the maximum allowable component spreads (see Fig. 4.5). The "bottom of the valley" in Fig. 4.4 is at x_∞ (see Fig. 4.6), given by

(4.11) $q_p(2\overline{\sigma}^2_R + 2\overline{\sigma}^2_C + \overline{\sigma}^2_{\alpha_v})x^4_\infty - (\overline{\sigma}^2_R + \overline{\sigma}^2_C + \overline{\sigma}^2_{\alpha_v})x^3_\infty$

$$+ \overline{\sigma}^2_{\alpha_v}x_\infty - q_p\overline{\sigma}^2_{\alpha_v} = 0 \,.$$

This equation was derived from (4.10a)–(4.10b) for $y \to \infty$. It can be used as a design equation, provided that the allowable component spread is large enough ($1/m^2 \gtrsim 10$ in our example).

Note that $x_\infty < 1$ for $m < 1$, which means that the resistor spread is always smaller than the capacitor spread. Finally, the gain α_V at the bottom of the valley is always less than 2, which will also be shown in the appendix on p. 75. This is an advantage, since the higher the gain of a voltage amplifier built using an opamp is, the higher are its noise and distortion, and the lower is its bandwidth.

<div style="text-align:right">*Upper limit on optimum gain*</div>

Unity-gain Sallen-and-Key low-pass filter   4.3.3

Sallen-and-Key filters are often built around an opamp connected as a unity-gain buffer. In this case, (4.3.2) can be solved for m:

<div style="text-align:right">*Reduce by one dimension*</div>

$$(4.12) \qquad m = \frac{n}{q_p(n^2+1)} \, .$$

It can be seen that $m \geq q_p/2$ for all possible n, which is a well-known result (cf. [Huelsman80]). For complex poles ($q_p > 0.5$), $m < 1$ and therefore $C_4 < C_2$. In other words, given a maximum allowable capacitor spread of $1/m^2$, only filters with $q_p \leq \frac{1}{2}m$ can be built.

Replacing m in all expressions by the term given in (4.12) amounts to mapping the white line in Fig. 4.7 onto a plane with constant m, giving a curve similar to those in Fig. 4.8. There remains only one degree of freedom, and the minimum-sensitivity filter can be found by solving $\nabla \overline{\sigma}_{q_p}^2 = 0$, which leads to the equation

<div style="text-align:right">*Calculate optimum n directly*</div>

$$(4.13) \quad 4\left(\overline{\sigma}_{\alpha_v}^2 q_p^4 - \overline{\sigma}_R^2\right)n^8 + 4\left(4\overline{\sigma}_{\alpha_v}^2 q_p^4 + \overline{\sigma}_R^2\right)n^6$$
$$+ 24\overline{\sigma}_{\alpha_v}^2 q_p^4 n^4 + 16\overline{\sigma}_{\alpha_v}^2 q_p^4 n^2 + 4\overline{\sigma}_{\alpha_v}^2 q_p^4 = 0$$

under the condition that $\overline{\sigma}_R^2$ and $\overline{\sigma}_C^2$ are identical for all resistors and capacitors, respectively. Note that the solution is independent of $\overline{\sigma}_C^2$. After the substitution $\overline{\sigma}_{\alpha_v}^2 = \overline{\sigma}_R^2 k_v^2/q_p^4$, this
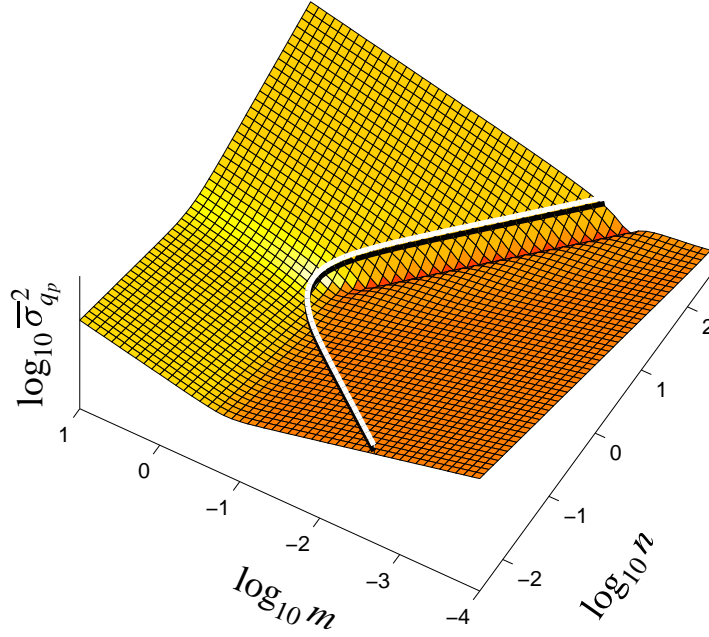
Figure 4.7   *Example of $\overline{\sigma}_{q_p}^2$ with the line on which $\alpha_V = 1$.*

equation becomes

(4.14) $\left(n^2 + 1\right)^4 k_v^2 - n^6 \left(n^2 - 1\right) = 0 \, .$

It can be seen that (4.14) can have one real root in the range $1 \leq n < \infty$, corresponding to $0 \leq k_v^2 < 1$ or

(4.15) $q_p^2 < \dfrac{\overline{\sigma}_R}{\overline{\sigma}_{\alpha_V}} \, .$

If condition (4.15) is not met, the minimum-sensitivity filter is again defined by the maximum allowable component spread, and the minimum achievable variance becomes $\frac{1}{2} q_p^2 (\overline{\sigma}_R^2 + \overline{\sigma}_C^2 + 2\overline{\sigma}_{\alpha_V}^2 q_p^4)$.

Examples

As an example, Fig. 4.8 shows $\overline{\sigma}_{q_p}^2$ for $\overline{\sigma}_R = \overline{\sigma}_C = 1\%$, $q_p = 3$ and $k_v = 2^{-11} \ldots 2^2$. It is apparent that the minimum normally occurs at $n \approx 1$, i.e. for a very small resistor spread, where $\overline{\sigma}_{q_p}^2$ is much smaller than it is for $n \gg 1$. It also appears that not much is to be gained if k_v is brought below 1/8.

To illustrate this, two numerical examples follow. Consider a low-pass filter with $q_p = 2$. Then a minimum exists for $\overline{\sigma}_{\alpha_V} < \frac{1}{4} \overline{\sigma}_R$. If 1 % resistors are used, the gain must not vary by
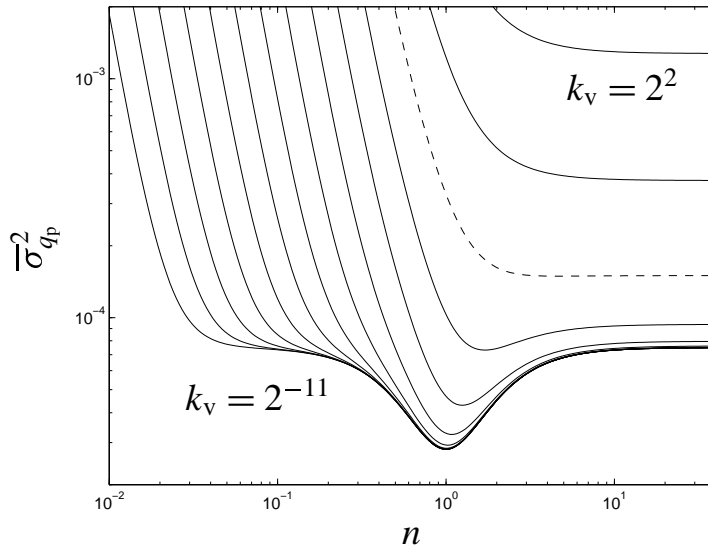
$\overline{\sigma}^2_{q_\mathrm{p}}$ *for different values of* k_v *(dashed:* $k_\mathrm{v} = 1$*).*   **Figure 4.8**
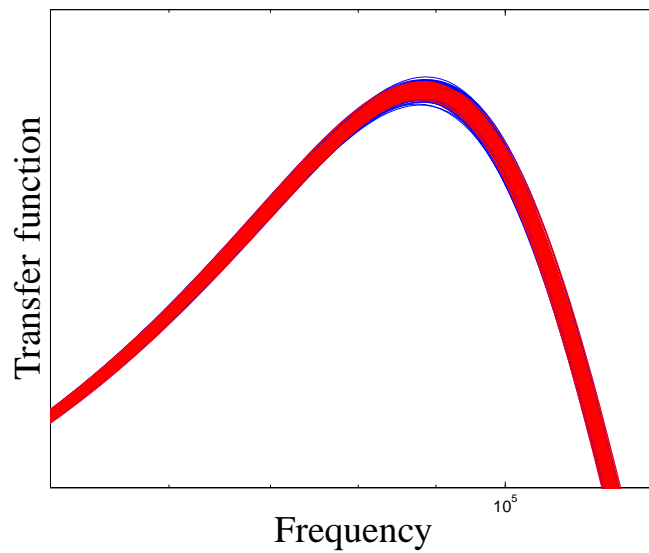
Monte-Carlo simulation for two filters having $q_\mathrm{p} = 1.5$ *and*   **Figure 4.9**
very large (black) and minimum (grey) component spreads.

more than 0.25 % (i.e. $\overline{\sigma}_{\alpha_V} < 0.0025$). The opamp's open-loop gain is approximately GBW/f, and therefore

$$(4.16) \qquad \overline{\sigma}_{\alpha_V} \approx \frac{f}{GBW} \overline{\sigma}_{GBW} \,,$$

where GBW is the Gain-Bandwidth Product of the opamp used to build the buffer. With $GBW = 1.5\,\text{MHz}$ and $\overline{\sigma}_{GBW} \approx 50\,\%$, which approximately describes the well-known LM 741, the filter should be built with low component spreads if it has a pole frequency f_p below 7.5 kHz. For a Butterworth or "maximally flat" filter (often used for anti-aliasing), $q_p = 1/\sqrt{2}$. Therefore $\overline{\sigma}_{\alpha_V} < 2\,\%$, and a minimum exists for all $f_p < 60\,\text{kHz}$.

Confirmed by simulation

All Monte-Carlo simulations we made confirm the theory. One example is shown in Fig. 4.9. It is obvious that the improvement in terms of $\overline{\sigma}_{q_p}^2$ is not large, but the real advantage in using small-spread filters is that higher pole frequencies can be realised using the same amplifier (c.f. Sec. 4.4).

4.3.4   Application to integrated filters

Extension

Up to here, the whole discussion was about discrete-component filters. We will now show that all results are also valid for integrated filters.

Use physically relevant sensitivities

On an IC, the physically relevant variations are not those of R_1, R_3, C_2 and C_4, but those of R and C, corresponding to the low-precision absolute values of the passive components, and m and n, corresponding to the highly precise component ratios. As mentioned above, the ratios of the passive components (or component spreads) are $\max\{n^2, 1/n^2\}$ and $\max\{m^2, 1/m^2\}$. It is not certain a priori whether n^2 or $1/n^2$ is greater than one. However, this does not matter, because as long as the variances are small, $\overline{\sigma}_{n^2}^2 \approx \overline{\sigma}_{1/n^2}^2$.

Compare discrete to integrated filters

Eq. (4.8) can now be written down for both discrete (a) and integrated (b) filters, assuming that $\overline{\sigma}_{R_1}^2 = \overline{\sigma}_{R_3}^2 = \overline{\sigma}_R^2$ and $\overline{\sigma}_{C_2}^2 = \overline{\sigma}_{C_4}^2 = \overline{\sigma}_C^2$:

$$(4.17a) \qquad \overline{\sigma}_{q_p}^2 \approx 2\overline{\sigma}_R^2 \left(S_{R_1}^{q_p}\right)^2 + 2\overline{\sigma}_C^2 \left(S_{C_2}^{q_p}\right)^2 + \overline{\sigma}_{\alpha_V}^2 \left(S_{\alpha_V}^{q_p}\right)^2 \,,$$

$$(4.17b) \qquad \overline{\sigma}_{q_p}^2 \approx \overline{\sigma}_{n^2}^2 \left(S_{n^2}^{q_p}\right)^2 + \overline{\sigma}_{m^2}^2 \left(S_{m^2}^{q_p}\right)^2 + \overline{\sigma}_{\alpha_V}^2 \left(S_{\alpha_V}^{q_p}\right)^2 \,.$$

The two expressions look very similar. It can be shown that

$$(4.18) \qquad S_n^{q_p} = -2 \cdot S_{R_1}^{q_p} \quad \Longrightarrow \quad S_{n^2}^{q_p} = -S_{R_1}^{q_p} ,$$

$$(4.19) \qquad S_m^{q_p} = -2 \cdot S_{C_2}^{q_p} \quad \Longrightarrow \quad S_{m^2}^{q_p} = -S_{C_2}^{q_p} .$$

Therefore (4.17a) and (4.17a) are identical if $\overline{\sigma}_{n^2}^2 = 2\overline{\sigma}_R^2$ and $\overline{\sigma}_{m^2}^2 = 2\overline{\sigma}_C^2$, and all results derived above also apply for integrated filters. Most importantly, the upper limit for the optimum gain of a Sallen-and-Key low-pass filter is still two.

Bandpass and high-pass filters   4.3.5

The same analysis can also be carried out for other Sallen-and-Key filters, giving similar results. The high-pass filter is dual to the low-pass filter, which means that the resistors and capacitors exchange their roles; but otherwise the results are the same as before. The results are slightly different for the two RC-dual bandpass filters, in which case the gain of the minimum-sensitivity filter is upper-bounded by four instead of two.

Appendix — proofs   4.3.6

Proof of the statement that the equation system (4.10a)–(4.10b) **has no solution for** $x > 0$, $y > 0$, $q_p > \frac{1}{2}$. Outline:

1. Calculate the root locus of (4.10a) for $0 \leq q_p \leq \infty$ and show that it has exactly one positive real root if $q_p > \frac{1}{2}$.
2. Express q_p as a function of x and show that y is negative over the whole range of x for $\frac{1}{2} < q_p < \infty$.

Part 1 — Rewrite (4.10a) as a polynomial in q_p:

$$(4.20) \quad q_p \left(2\overline{\sigma}_R^2 (2\overline{\sigma}_C^2 + \overline{\sigma}_{\alpha_v}^2) x^4 - 2\overline{\sigma}_C^2 \overline{\sigma}_{\alpha_v}^2 \right) -$$
$$\left(\overline{\sigma}_R^2 (2\overline{\sigma}_C^2 + \overline{\sigma}_{\alpha_v}^2) x^3 - \overline{\sigma}_C^2 \overline{\sigma}_{\alpha_v}^2 x \right) = 0 .$$

The four roots can be calculated at three special points:

q_{p}	Roots	(Finite) Positive Real Root
0	$0, (k_\sigma)^{\frac{1}{2}}, \infty$	$x\mid_{q_{\mathrm{p}}=0} = \sqrt{k_\sigma}$
$\frac{1}{2}$	$1, (-k_\sigma)^{\frac{1}{3}}$	$x\mid_{q_{\mathrm{p}}=\frac{1}{2}} = 1$
∞	$(k_\sigma)^{\frac{1}{4}}$	$x\mid_{q_{\mathrm{p}}=\infty} = \sqrt[4]{k_\sigma}$

$$(4.21) \qquad \text{with} \qquad k_\sigma = \frac{\overline{\sigma_C^2}\,\overline{\sigma_{\alpha_v}^2}}{\overline{\sigma_R^2}(2\overline{\sigma_C^2} + \overline{\sigma_{\alpha_v}^2})} .$$

There are only two fundamentally different root locii:

condition	x for $\infty > q_{\mathrm{p}} > \frac{1}{2}$
$k_\sigma < 1$	$\sqrt[4]{k_\sigma} < x < 1$
$k_\sigma > 1$	$\sqrt[4]{k_\sigma} > x > 1$

One example of each is shown in Fig. 4.10. The theory of root locii says that, for varying q_{p}, the roots move from the roots for $q_{\mathrm{p}} = 0$ (circles) to the roots for $q_{\mathrm{p}} \to \infty$ (crosses). It also follows from the theory, for both types of root locus occurring here, that the two roots that leave the real axis cannot return to the real axis and leave again. Thus the fact that there is only one positive real root for $q_{\mathrm{p}} = \frac{1}{2}$ proves that the same is also true for all $q_{\mathrm{p}} > \frac{1}{2}$. (Note that there is also a range of values for q_{p} below $\frac{1}{2}$ for which there is only one positive real root, but this is of no interest for our proof.)

Part 2:—Express q_{p} as a function of x:

$$(4.22) \qquad q_{\mathrm{p}} = \frac{\overline{\sigma_R^2}(2\overline{\sigma_C^2} + \overline{\sigma_{\alpha_v}^2})x^3 + \overline{\sigma_C^2}\,\overline{\sigma_{\alpha_v}^2}\,x}{2\overline{\sigma_R^2}(2\overline{\sigma_C^2} + \overline{\sigma_{\alpha_v}^2})x^4 - 2\overline{\sigma_C^2}\,\overline{\sigma_{\alpha_v}^2}} .$$

Substitute (4.22) into equation (4.10b):

$$(4.23) \qquad y = \frac{x}{\overline{\sigma_{\alpha_v}^2}} \cdot \frac{\overline{\sigma_R^2}(2\overline{\sigma_C^2} + \overline{\sigma_{\alpha_v}^2})x^2 - \overline{\sigma_C^2}\,\overline{\sigma_{\alpha_v}^2}}{\overline{\sigma_R^2}x^4 + (\overline{\sigma_C^2} - \overline{\sigma_R^2})x^2 - \overline{\sigma_C^2}} .$$

Both numerator and denominator have exactly one positive real root, namely $\sqrt{k_\sigma}$ and 1. There are two possibilities:

$k_\sigma < 1$: $y < 0$ for $\sqrt{k_\sigma} < x < 1$. Since $\sqrt{k_\sigma} < \sqrt[4]{k_\sigma}$, this range contains all x for $\frac{1}{2} < q_{\mathrm{p}} < \infty$, and there is no solution to the optimisation problem.

$k_\sigma > 1$: $y < 0$ for $\sqrt{k_\sigma} > x > 1$. For the same reason as before, there is no solution to the optimisation problem.

Proof of the statement that the gain of the minimum-sensitivity filter does not exceed 2.

Figure 4.6 shows the same example as Fig. 4.4 including the lines on which the gradients in the directions of the m and n axes are zero. For $y \gg 1$, these lines converge towards the same x-value x_∞, which is described by (4.11) above. As before, a root locus analysis can be made:

$$x_\infty|_{q_p=0} = \sqrt{k_{\sigma 0}} \qquad k_{\sigma 0} = \frac{\overline{\sigma}_{\alpha_v}^2}{\overline{\sigma}_R^2 + \overline{\sigma}_C^2 + \overline{\sigma}_{\alpha_v}^2}$$

$$x_\infty|_{q_p=\frac{1}{2}} = 1$$

$$x_\infty|_{q_p=\infty} = \sqrt[4]{k_{\sigma \infty}} \qquad k_{\sigma \infty} = \frac{\overline{\sigma}_{\alpha_v}^2}{2\overline{\sigma}_R^2 + 2\overline{\sigma}_C^2 + \overline{\sigma}_{\alpha_v}^2}$$

This time, there is only one type of root locus, since $\sqrt{k_{\sigma 0}} < \sqrt[4]{k_{\sigma \infty}} < 1$ for all choices of $\overline{\sigma}_R^2, \overline{\sigma}_C^2, \overline{\sigma}_{\alpha_v}^2$. It has the same form as the one at the top of Fig. 4.10. Therefore it follows that

$$(4.24) \quad \left(\frac{\overline{\sigma}_{\alpha_v}^2}{2\overline{\sigma}_R^2 + 2\overline{\sigma}_C^2 + \overline{\sigma}_{\alpha_v}^2} \right)^{\frac{1}{4}} < x_\infty < 1 \quad \text{for } \infty > q_p > \frac{1}{2},$$

and x_∞ is always smaller than unity. It follows from equation (4.9) that the sensitivity is minimum at an $n < \frac{1}{m}$ for large n. Thus the filter should have high component spreads, where the capacitor spread is always greater (but normally not much greater) than the resistor spread.

Equation (4.3.2) is now translated into x, y coordinates, and the limit $y \gg 1$ is taken. Solved for q_p:

$$(4.25) \qquad\qquad q_p = \frac{x}{x^2 + 1 - \alpha_V} \,.$$

Substitute (4.25) into (4.11), and solve for α_V:

$$(4.26) \qquad \alpha_V = -x^2 \frac{(\overline{\sigma}_R^2 + \overline{\sigma}_C^2)x^2 - (\overline{\sigma}_R^2 + \overline{\sigma}_C^2)}{(\overline{\sigma}_R^2 + \overline{\sigma}_C^2 + \overline{\sigma}_{\alpha_v}^2)x^2 - \overline{\sigma}_{\alpha_v}^2} \,.$$

This function has four zeros $(-1, 0, 0, 1)$ and two poles $(\pm\sqrt{k_{\sigma 0}})$, thus it is positive over the whole range of x. It

is also monotonically increasing from $\alpha_V = 0$ for $q_p = \frac{1}{2}$ up to $\alpha_V = 1 + \sqrt{k_{\sigma\infty}}$ for $q_p \to \infty$, and can therefore not be greater than 2.
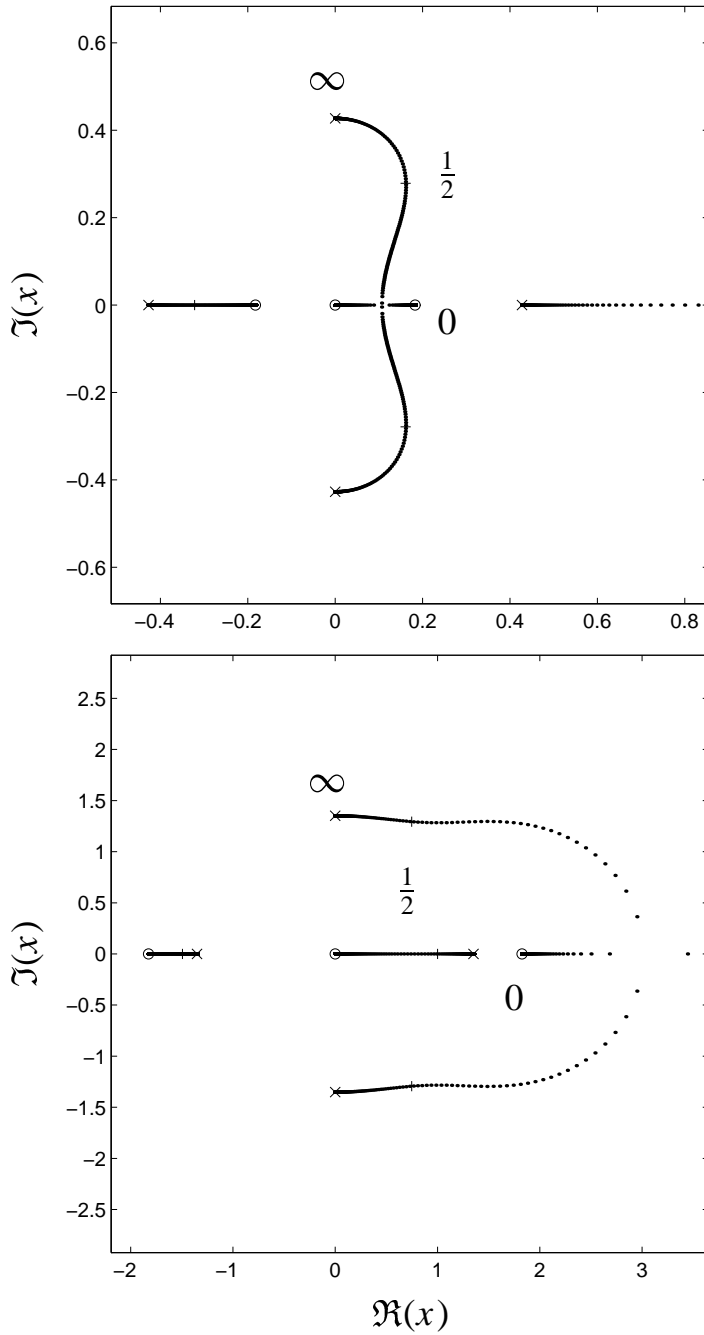
Root locii for $\overline{\sigma}_C^2 = \overline{\sigma}_{\alpha_v}^2 = 0.1\,\overline{\sigma}_R^2$ (top) and $\overline{\sigma}_C^2 = \overline{\sigma}_{\alpha_v}^2 = 10\,\overline{\sigma}_R^2$ (bottom). 'o' are the roots for $q_p = 0$, '+' for $q_p = \frac{1}{2}$ and '×' for $q_p \to \infty$.
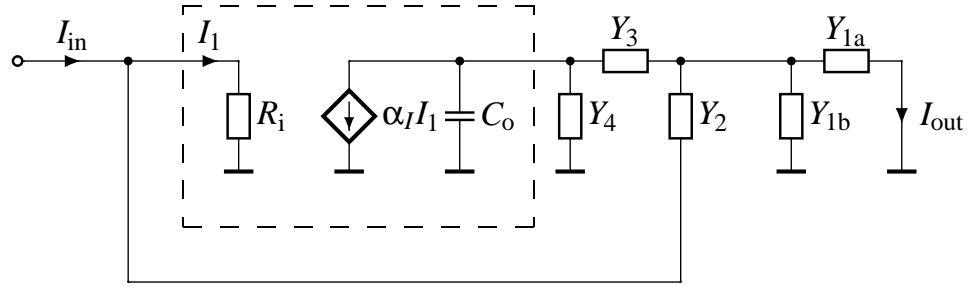
Figure 4.10

Figure 4.11   *Sallen-and-Key filter structure (LP, BP and HP).*

4.4   Amplifier non-idealities

Amplifier phase model

As was shown in Sec. 3.4.2, the properties of open-loop amplifiers and of high-gain amplifiers with feedback are not all that different when the operating frequency is pushed to the limits. Especially the linear phase-lag model used in this section is valid for both. We will discuss only the influence of non-idealities of open-loop amplifiers on Sallen-and-Key, but the discussion can easily be applied to high-gain amplifiers with feedback as well, with similar results.

4.4.1   Current-mode Sallen-and-Key filters

Terminal impedance model

Fig. 4.11 shows a general current-mode Sallen-and-Key filter structure which can be used to implement a low-pass (LP), two different bandpass (BP1, BP2) and a high-pass (HP) second-order transfer function. The Sallen-and-Key filter in Fig. 4.11 is built around a low-gain current amplifier with finite input admittance (R_i, resistive) and low, but not zero output admittance (C_o, capacitive). Although a current amplifier has been chosen in this section, the same analysis is also valid for a voltage amplifier with input capacitance C_o and output resistance R_i [Moschytz94]. Note that the gain α_I of the current amplifier must be negative in order to produce positive feedback (c.f. Sec. 3.3).

Using geometrical means and aspect ratios

Table 4.2 shows how the admittances in Fig. 4.11 have to be chosen in order to realise the three different filter functions. The resistors and capacitors are expressed in terms of geometrical means (R, C) and component spread factors (m, n), because this

	Y_{1a}	Y_{1b}	Y_2	Y_3	Y_4	R_i	C_o
LP	R/n	0	C/m	Rn	Cm	R/ρ	C/κ
BP1	C/m	R/n	C/m	Rn	Cm	R/ρ	C/κ
BP2	R/n	C/m	R/n	Cm	Rn	R/ρ	C/κ
HP	C/m	0	R/n	Cm	Rn	R/ρ	C/κ

Filter components. **Table 4.2**

leads to independent expressions for the *ideal* pole frequency ω_{pi} and the *ideal* pole quality factor q_{pi}. The amplifier's non-ideal port admittances are expressed in terms of R, C and of the impedance level factors $\rho = R/R_i$ and $\kappa = C/C_o$, which would be infinite for an ideal amplifier.

Low-gain amplifiers normally do not have one dominant pole, but a cluster of poles and zeros at high frequencies. Thus there is no general physical model for the amplifier's phase-lag that is valid over the whole frequency range of interest. Nevertheless, if the phase lag of the amplifier at the filter's pole frequency is reasonably small (say around 10…20 degrees), its effects on the pole location can be approximated by using a linear phase lag (constant group delay) model. Then

Linear phase-lag model

$$(4.27) \qquad \alpha_I(s) = \alpha_{I(s=0)} \cdot e^{(-\phi RCs)} .$$

Here s is the complex frequency normally written as $s = \sigma + j\omega$, and ϕ is the phase lag at $\omega = 1/(RC)$, which is the pole frequency of the LP and HP filters, and close to the pole frequencies of the two BP filters (see equations (4.28_{LP})–(4.28_{HP})). The resulting non-linear filter transfer function can be linearised by setting $\phi = 0$ in the numerator (this must be done, because the phase lag model is only accurate in the region of the pole frequency, but not around the frequencies of the zeros) and by expanding the denominator as a Taylor series in s, cancelling all terms of order 3 and higher. This approximated filter transfer function allows a prediction of the shift of ω_p and q_p for all amplifier non-idealities, as given in the next section.

4.4.2   Pole shifts

Poles of the LP filter   Ideally, the poles of the LP filter lie at

$$(4.28_{\text{LP}}) \qquad (\omega_{\text{pi}}, \frac{1}{q_{\text{pi}}}) = \left(\frac{1}{RC}, \frac{m^2n^2 + m^2 + (\alpha_{\text{I}} + 1)}{mn} \right).$$

The equations for the bandpass and high-pass filters can be found in the Appendix on p. 87. The pole quality factor of (4.28_{LP}) can be written as

$$\frac{1}{q_{\text{pi}}} = \frac{1}{mn} + mn + \frac{1}{n} \left(\frac{\alpha_{\text{I}}}{m} + m \right).$$

Rules for choosing m and n

It can easily be seen that $1/mn + mn \geq 2$, with equality for $mn = 1$. q_{pi} can be made larger than $1/2$ only if $1/n \cdot (\alpha_{\text{I}}/m + m)$ is negative, which is the case for $m < \sqrt{-\alpha_{\text{I}}}$,[1] and since $|\alpha_{\text{I}}|$ should not become too high, n should also be limited. In practice, m and n should be chosen such that $mn \approx 1$, $m \lesssim 1$, and n is reasonably small (on the order of unity). Similar rules for choosing m and n can be derived for the other filters. From (4.28_{BP1}): $mn \approx \sqrt{2}$ and $m \lesssim 1$ for a reasonably small n. From (4.28_{BP2}): $mn \approx 1/\sqrt{2}$ and $n \gtrsim 1$ at a reasonably large m (on the order of unity). From (4.28_{HP}): $mn \approx 1$ and $n \gtrsim 1$ at a reasonably large m.

Shifted pole frequency and pole Q

The three non-idealities (finite R_{i}, non-zero C_{o} and non-zero ϕ) shift the poles towards lower frequencies, where

$$(4.29_{\text{LP}}) \qquad \frac{\omega_{\text{p}}^2}{\omega_{\text{pi}}^2} = \frac{\rho\kappa mn}{\rho\kappa(mn - \phi\alpha_{\text{I}}) + \rho n + (\kappa m + 1)(n^2 + 1)}.$$

The pole quality factors can also be expressed in terms of ρ, κ and ϕ, but here it is less obvious what happens to q_{p}:

$$(4.30_{\text{LP}})$$
$$\frac{1}{q_{\text{p}}} = \frac{\rho\kappa(m^2n^2 + m^2 + (\alpha_{\text{I}} + 1)) + \rho m(n^2 + 1) + \kappa n}{\sqrt{\rho\kappa mn}\sqrt{\rho\kappa(mn - \phi\alpha_{\text{I}}) + \rho n + (\kappa m + 1)(n^2 + 1)}}.$$

---

[1] Remember that $\alpha_{\text{I}} < 0$.

If $\phi = 0$ and either ρ or κ is assumed infinite, all expressions (4.30_{LP})–(4.30_{HP}) can be brought into the form

$$\frac{1}{q_{\mathrm{p}}} = \frac{1}{q_{\mathrm{pi}}} \cdot k_1 + k_2$$

where $k_1 < 1$ and $k_2 > 0$. It can be seen that $k_1 \approx 1$ for small component spreads, therefore non-ideal amplifier port impedances normally *decrease* the pole quality factor q_{p}. On the other hand, an amplifier phase lag *increases* the pole quality factor. This behaviour has also been observed in Gm–C filters [Hung97].

Parasitic zeros   4.4.3

There is a non-ideal effect which affects filter performance more than the predictable and therefore compensatable pole shifts, namely the parasitic zero or zeros caused by a finite ρ.

$(4.31_{\mathrm{LP,BP1}})$

$$\left(\omega_{\mathrm{z}}^2, q_{\mathrm{z}} \right) = \left(\frac{1}{R^2 C^2} \frac{-\rho \alpha_{\mathrm{I}} m}{n \left(m + \frac{1}{\kappa} \right)}, \sqrt{-\rho \left(m + \frac{1}{\kappa} \right) \alpha_{\mathrm{I}} mn} \right),$$

$(4.31_{\mathrm{HP,BP2}})$

$$\omega_{\mathrm{z}} = \frac{1}{RC} \frac{1}{mn + \frac{n}{\kappa} - \rho \alpha_{\mathrm{I}} m} \ .$$

The effects on the filter transfer function differ:

Low-pass filter (LP). The complex pair of zeros causes the transfer function (TF) to become constant for frequencies above ω_{z}, and the minimum stopband attenuation A_{stop}, with respect to the passband attenuation A_{pass}, becomes $A_{\mathrm{stop}}/A_{\mathrm{pass}} \approx -\rho \alpha_{\mathrm{I}}/n$ (for $\kappa \gg 1/m$). Since α_{I} and n are normally on the order of unity, this means that $\rho = R_{1\mathrm{a}}/R_{\mathrm{i}}$ must be larger than the required stopband attenuation.

For a given pole frequency, the product RC must be constant. Making $R_{1\mathrm{a}} = R/n$ larger (for the same n) therefore means making C smaller. The ultimate limit is $C m = C_{\mathrm{o}}$, but this limit should not be approached, since Y_4 is then only a rather non-linear amplifier output capacitance.

<table>
<tr><td>

Limit on the
maximum pole
frequency

</td><td>

The resistance of the low-impedance terminal therefore imposes fundamental limitations on the filter's pole frequency, and the highest achievable frequency for a given stopband attenuation is

</td></tr>
</table>

$$(4.32) \qquad \omega_{p\,max} \approx \frac{A_{pass}}{\max(m, 1/m)C_o \cdot \max(n, 1/n)R_i \cdot A_{stop}} \, ,$$

which reaches a maximum at $m = n = 1$. Since the capacitors Y_4 and Y_2 must match well, Y_4 should not consist of parasitic capacitance only, and $\omega_{p\,max}$ should therefore not be approached too closely.

Bad high-frequency behaviour

Bandpass filter (BP1). Here the complex pair of zeros causes the TF to *rise 20 dB per decade* at frequencies above ω_z, until it flattens out again, at a gain of 1, because of a third high-frequency pole, which was cancelled from the Taylor series during the simplifications made above. Since ω_z/ω_p is in the order of $\sqrt{\rho}$, the filter's gain reaches unity at a frequency of about $\rho\omega_p$. *This may well make the filter useless for practical applications.*

Higher $\omega_{p\,max}$ than BP1

Bandpass filter (BP2). The single zero makes the TF constant for frequencies below ω_z, at a magnitude of approximately $\sqrt{2}\,\rho m$. Here it is a matter of convenience and interpretation to which level this should be referred, but the same fundamental frequency limitations occur as in the LP case.

No closed-form design expressions

High-pass filter (HP1). In this case, the single zero changes the slope of the TF from 40 dB per decade to 20 dB per decade for frequencies below ω_z. Again, the minimum capacitance to be used in the feedback network and the filter specifications impose frequency limitations, although in this case the dependence of the maximum frequency on the specifications is more complicated and is best evaluated graphically or numerically.

Examples

To clarify the above discussion, Fig. 4.12 shows the transfer functions of all four filters, where $m = 0.6$, $n = 1$, $\alpha_I = -1.6$, $\kappa = 30$ and $\rho = 10, 30, 100$. The magnitudes of HP and BP2 have been multiplied by 4, and different pole frequencies have been chosen, both for graphical reasons only. The effects of the parasitic zeros can be seen clearly in all four cases. It is also evident that the LP filter has by far the highest q_{pi}, which already follows from (4.28_{LP})–(4.28_{HP}).
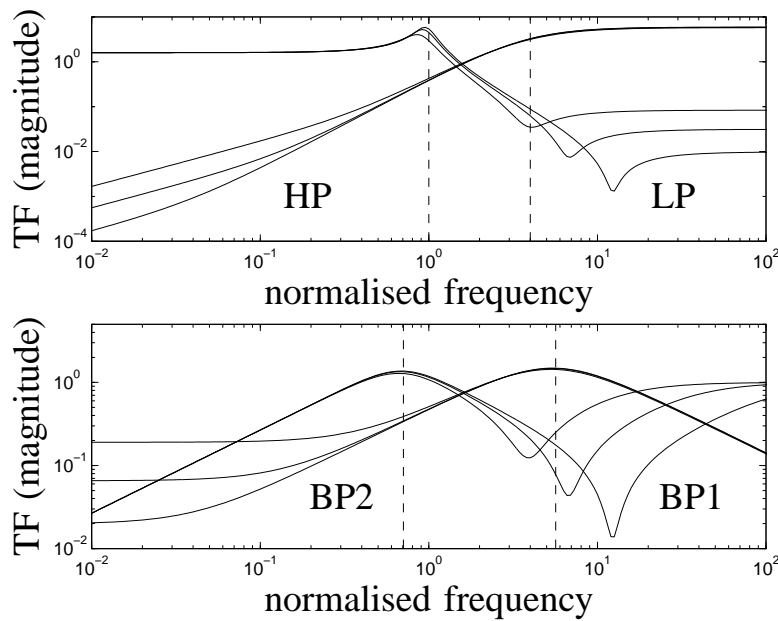
Transfer functions (TF) of the LP, BP1, BP2 and HP filters.
The dashed lines indicate the different ω_{pi}.

Figure 4.12

Practical example

4.4.4

As an example, consider a Sallen-and-Key low-pass filter bi-quad with $f_\mathrm{p} = 16.58\,\mathrm{MHz}$, $q_\mathrm{p} = 4$, and a stopband attenuation of at least $30\,\mathrm{dB}$.[2]

Filter with medium q_p

A single-ended CMOS class AB second-generation current conveyor (CCII) is used as current amplifier. It is similar to the balanced CCII presented in [Schmid97], which is the balanced variant of the CCII shown in Fig. 2.10. Simulations show that the current input of the CCII has a resistance on the order of $100\,\Omega$, depending on the bias current, while the current output has a capacitance of $C_\mathrm{o} \approx 0.05\,\mathrm{pF}$.

The choice of "optimum" values of m, n and α_I really depends on which sensitivity criterion should be optimised (c.f. Sec. 4.3). Here we choose reasonable values according to the criteria given in Section 4.4.2 without further explanation: neglecting the passband attenuation ($A_\mathrm{pass} \approx 0\,\mathrm{dB}$), and assuming $\max(m, 1/m) \approx 2$ and $\max(n, 1/n) \approx 1.25$, it follows that the input resistance of the CCII must be $R_\mathrm{i} = 240\,\Omega$. Then

Choose α_I, m and n

---

[2]Although it is rather small, this attenuation already results in $60\,\mathrm{dB}$ stopband attenuation for a cascade of two biquads in a 4th-order filter.

	simulated	corrected	ideal
f_p [MHz]	13.6 (-18%)	16.2 (-2%)	16.58
q_p	3.0 (-25 %)	3.9 (-2.5 %)	4.0

Table 4.3   *Simulated ω_p and q_p of the LP transfer function.*

$C = \max(m, 1/m)\, C_o = 1\,\text{pF}$, and $R = 9.6\,\text{k}\Omega$ from (4.28$_{\text{LP}}$). The CCII used for the simulations has a gain of $\alpha_I = -1.57$. If $n = 1$ is chosen, as suggested in the previous section, it follows that $m = 0.6$. However, if the filter is built using these values, the actual pole frequency and pole quality factor will deviate from the ideal. Since the CCII has a phase lag of 7 degrees at 16.58 MHz, the equations (4.29$_{\text{LP}}$) and (4.30$_{\text{LP}}$) predict $f_p = 13.6\,\text{MHz}$ and $q_p = 3.1$. This corresponds well to the simulated $f_p = 13.6\,\text{MHz}$ and $q_p = 3.0$.

Correcting ω_p

The pole frequency can be corrected by making R smaller, either in two or three iterative steps, or by replacing ρ by R/R_i in (4.29$_{\text{LP}}$) and solving for R. This results in $R = 7.85\,\text{k}\Omega$ (and therefore $\rho = 32.7$). Due to other non-ideal effects, the pole frequency $f_p = 16.2\,\text{MHz}$ is still slightly low, but close enough such that a new value for $1/R$ can be linearly extrapolated,[3] resulting in $R = 7.58\,\text{k}\Omega$ and a filter having the correct f_p.

Correcting q_p

The problem of the low q_p remains. A similar procedure can now be applied to (4.29$_{\text{LP}}$), solving for a new value of $n = 0.9$. Now the simulated filter has a $q_p = 3.9$, but f_p has not been changed, since the two are orthogonal to each other. Linear extrapolation suggests using $n = 0.89$, which gives the correct q_p.

Discussion

Table 4.3 shows the ideal values of f_p and q_p and the simulated values with ideal components ("simulated") and with components calculated using equations (4.29$_{\text{LP}}$) and (4.30$_{\text{LP}}$) ("corrected"). The values after linear interpolation are not shown, since they differ from the ideal values by less than 0.2%. The stopband attenuation of the filter reaches its maximum of 35 dB at about 400 MHz, which is better than expected. The reason for this unexpected improvement is that the gain of the CCII has already decreased by 7 dB at this frequency.

---

[3]Note that f_p is a linear function of $1/R$, not R.

This example shows that the equations (4.29$_{\text{LP}}$) and (4.30$_{\text{LP}}$) themselves provide a very good means of designing a filter, even if only R_i, C_o and the phase lag at f_p of the amplifier are known, and no accurate simulations of the whole filter can be made. Non-idealities of the CCII other than input resistance, output capacitance and phase lag, e.g. attenuation at high frequencies or parasitic poles and zeros in the impedances, can also be accounted for if the whole filter can be simulated and one additional interpolation step is made.

<div style="float:right; text-align:right; font-style:italic;">
Deterministic compensation of amplifier non-idealities is good enough
</div>

Appendix 4.4.5

(4.28$_{\text{BP1}}$) $\quad (\omega_{\text{pi}}, \dfrac{1}{q_{\text{pi}}}) = \left(\dfrac{1}{\sqrt{2}\,RC}, \dfrac{m^2 n^2 + m^2 + (\alpha_\text{I}+2)}{\sqrt{2}\,mn} \right) ,$

(4.28$_{\text{BP2}}$) $\quad \left(\dfrac{\sqrt{2}}{RC}, \dfrac{m^2 n^2(\alpha_\text{I}+2) + m^2 + 1}{\sqrt{2}\,mn} \right) ,$

(4.28$_{\text{HP}}$) $\quad \left(\dfrac{1}{RC}, \dfrac{m^2 n^2(\alpha_\text{I}+1) + m^2 + 1}{mn} \right) .$

(4.29$_{\text{BP1}}$) $\quad \dfrac{\omega_\text{p}^2}{\omega_{\text{pi}}^2} = \dfrac{\rho\kappa mn}{\rho\kappa(mn - \frac{1}{2}\phi\alpha_\text{I}) + \rho n + \frac{1}{2}(\kappa m + 1)(n^2 + 1) + \frac{\kappa}{2m}} ,$

(4.29$_{\text{BP2}}$) $\quad \dfrac{\rho\kappa mn + \frac{\kappa mn^2}{2}}{\rho\kappa(mn - \phi m^2 n^2 \alpha_\text{I}) + (\rho n + n^2)(m^2 + 1) + \kappa mn^2} ,$

(4.29$_{\text{HP}}$) $\quad \dfrac{\rho\kappa mn}{\rho\kappa(mn - \phi m^2 n^2 \alpha_\text{I}) + (\rho n + n^2)(m^2 + 1) + \kappa mn^2} ,$

(4.30$_{\text{BP1}}$)

$$\dfrac{1}{q_\text{p}} = \dfrac{\rho\kappa(m^2 n^2 + m^2 + (\alpha_\text{I}+2)) + \rho m(n^2 + 1) + \kappa n}{\sqrt{\rho\kappa mn}\sqrt{\rho\kappa(2mn - \phi\alpha_\text{I}) + 2\rho n + \kappa m(n^2 + 1) + \frac{\kappa}{m} + (n^2 + 1)}} ,$$

(4.30$_{\text{BP2}}$) $\quad \dfrac{\rho\kappa(m^2 n^2(\alpha_\text{I}+2) + m^2 + 1) + 2\rho mn^2 + \kappa n(m^2 n^2 + m^2 + 1) + mn^3}{\sqrt{(2\rho + n)\kappa mn}\sqrt{\rho\kappa(mn - \phi\alpha_\text{I} m^2 n^2) + \rho n(m^2 + 1) + n^2(m^2 + \kappa m + 1)}} ,$

(4.30$_{\text{HP}}$) $\quad \dfrac{\rho\kappa(m^2 n^2(\alpha_\text{I}+1) + m^2 + 1) + \rho mn^2 + \kappa n(m^2 + 1)}{\sqrt{\rho\kappa mn}\sqrt{\rho\kappa(mn - \phi\alpha_\text{I} m^2 n^2) + \rho n(m^2 + 1) + \kappa mn^2 + n^2(m^2 + 1)}} .$

4.5   Conclusion

More theory is
not necessary

The preceding sections establish the main points of theory that are necessary to design active-RC SABs. In our opinion, the above theory is sufficient, since an actual design will be carried out in simulation–re-design cycles anyway after an initial calculation. It is mainly the qualitative aspects that should be kept in mind when designing filters like the ones in the following Part II.

Part II

The Transistor Level

Chapter 5

Second-order MOSFET–C networks

**What every organisation needs
is one damn fool
who doesn't know what you can't do.**

(Sir Robert Watson-Watt)

The main points of this Chapter are to show what happens when the MOSFET–C technique is applied to single-amplifier biquadratic filters (SABs), and to give a few design guidelines. A brief introduction explains where this idea comes from; it is followed by a section on transistor models where it is shown that bulk-referenced transistor models would be needed to simulate MOSFET–C filters properly, and that the unconventional operating conditions of MOSFET resistors should be taken into account when the model parameters are extracted.

It is then shown how the analogue ground should be chosen in second-order MOSFET–C networks in order to minimise the total harmonic distortion (THD). The next section discusses the possibility of controlling the MOSFET resistors with a voltage generated by a charge pump, and it is shown how the maximum signal swing should be set to minimise the signal-to-noise ratio. Finally, various influences on the THD are discussed, and the possibility of building MOSFET-only filters is briefly looked at. An appended section discusses various ways to measure and simulate harmonic distortion.

5.1   Background

Since tuning the pole frequency of an SAB requires adjusting the values of passive components, I had to stumble over MOSFET resistors sooner or later. The way it happened was that I bought [Tsividis93] on the recommendation of a friend. I immediately saw that MOSFET resistors would enable me to integrate SABs. The other possibilities would have been to tune the filter in steps by switching capacitors on and off, or by using variable capacitors, but both possibilities never appealed to me, because both were far less straightforward than the MOSFET–C technique. So the main reasons why I concentrated on MOSFET–C filters was their simplicity and intellectual beauty.

I was very lucky that I had not found [Czarnul88] before my first chip was already made, because there it is stated explicitly that Sallen-and-Key filters should not be built as MOSFET–C filters because they cause too much harmonic distortion. I think that this would have discouraged me, because back then I would certainly not have seen the qualitative difference between building the audio-frequency 100 dB-SFDR from [Czarnul88] and my video-frequency, 50 dB-SFDR filters that I explain below.

During my research, I found that the harmonic distortion in my filters was quite high [Schmid99b, Schmidood]. When I read [Duisters98], however, I immediately saw that the THD of my filters would improve very much if I used a charge pump to generate the control voltage of the MOSFET resistors. I built such filters on my second chip, and published one in [Schmidooe].

5.2   Introduction to MOSFET–C filters

Integrated active-RC integrators with adjustable time constant

The concept of MOSFET–C filters was first introduced in 1983 [Banu83] to make the integration of active-RC filters on integrated circuits possible. The problem with integrating the conventional active-RC integrator is that its time constant
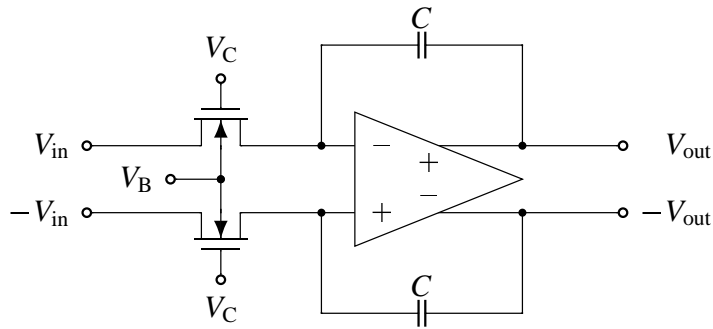
Banu-Tsividis integrator   **Figure 5.1**

depends on the values of passive elements only. In order to adjust the time constant of such an integrator, one needs to adjust the values of the passive components.

The solution proposed by Banu and Tsividis in [Banu83] is to replace the resistors in the active-RC integrator by MOSFETs operating in the linear region, as shown in Fig. 5.1. This introduces harmonic distortion, but since the distortion is mainly of second order, it can be cancelled completely (in theory) by using a balanced design like the one in Fig. 5.1.

Replace resistors by MOSFETs

One disadvantage of this structure is that a balanced-output opamp has to be used. It is also possible to build MOSFET–C integrators with conventional (single-output) opamps if a MOS resistive network comprising four matched transistors is used [Czarnul86], but the disadvantage of this technique is that two different gate control voltages are then necessary. Non-linearity cancellation can also be achieved using techniques that are slightly different from the one portrayed in Fig. 5.1; a good overview can be found in [Tsividis86].

Other ways to build MOSFET–C integrators

The harmonic distortion that remains at the output of a MOSFET–C integrator has been meticulously calculated in [Banu84]. However, even for this simple case, the calculations are very tedious and can only be carried out with several simplifications. We made several attempts to do a similar calculation for higher-order MOSFET–C networks, but always failed because the equations became very complex.

Mathematical analysis is very difficult

Fortunately, such a detailed analysis is not really needed for the design of video-frequency MOSFET–C filters. If the design target is a total harmonic distortion (THD) between

Clipping is more prominent than soft distortion

−40 and −50 dB, then the calculations and comments made in [Czarnul88, Banu84] are not really relevant, because there only the curvature of the MOSFET resistor characteristic is considered, whereas the main contribution to a THD of that magnitude comes from signal clipping.

Overview

Thus we will restrict all mathematical discussions to evaluating the effect of clipping and give a more detailed account of what happens in a second-order MOSFET–C network by presenting simulation results. We will first do this for a conventional biquadratic MOSFET–C filter, and then we will discuss what changes if the gate control voltage is generated using a charge pump. We will then briefly discuss the possibility of building MOSFET–only filters, i.e., to implement our MOSFET–C filters on silicon processes that do not provide poly-poly capacitors. But first we will discuss a few important aspects of transistor models, parameters, and the simulation of MOSFET–C filters.

5.3   A note on transistor models

The models and the parameters must be suitable

The transistor models that we used for designing our MOSFET–C filters were far from ideal for the task. The problem with today's CMOS transistor models is that both the model equations and the model parameters must be suitable for the simulation of the circuit at hand.

Bulk-referenced models should be used to simulate MOSFET–C filters

This can be shown very easily for the model equations. Two transistor models are supplied with the AMS 0.6-μm process we used, the Spectre Level 53 model, which is the BSIM 3v3 V.1 model, and the Spectre Level 15 model, which is AMS's own transistor model. Both models are source-referenced, which means that all terminal voltages are referred to the source terminal. This is not really suitable for modelling MOSFET resistors, since if the current through the transistor changes its direction, then source and drain are exchanged, and discontinuities may result. For example, Fig. 5.2 shows simulations made with both models of an nMOS resistor of the size 12×6.9 μm, which corresponds to the serial connection of both nMOS resistors in the charge-pump controlled biquad described in Sec. 7.4.2. One terminal was connected to analogue ground, $V_S = 0$ V, and the voltage V_D of the other
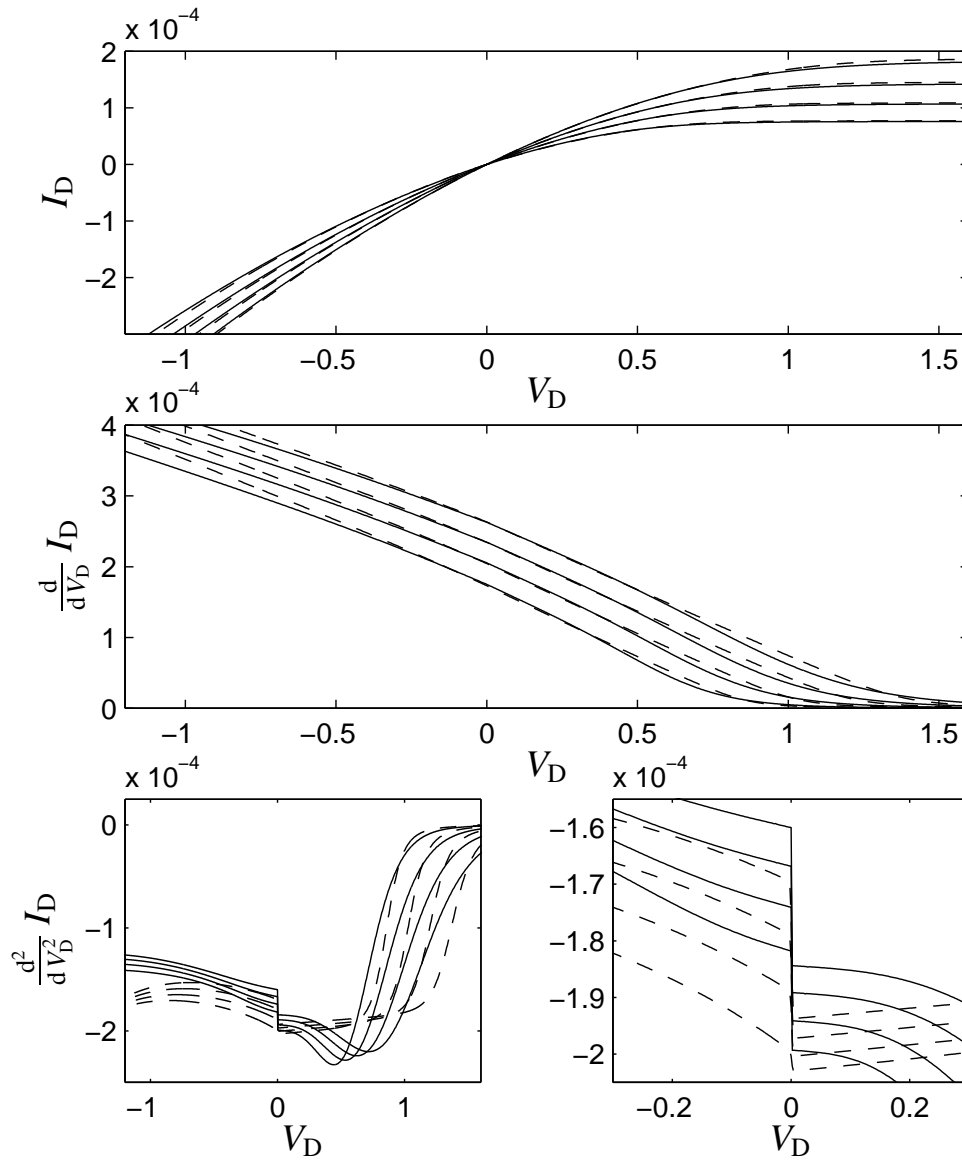
*Comparison of the Spectre Level 15 model (solid lines) and
the Level 53 model (dashed lines).*

Figure 5.2

terminal was varied. Fig. 5.2 contains plots of the drain current I_D and its first and second derivative, for four gate voltages in the range of 4.0 V to 4.6 V. Both models show a discontinuity in the second derivative at $V_D = 0$, which means that the first derivative, the differential resistance, is not smooth in the operating point of the MOSFET–C filter.

Model parameters must be extracted with this application in mind

It is also very important to have good model parameters.[1] Most CMOS transistor models used today have only very few physical parameters, the majority of parameters are used for fitting curves to measurements. This means, among other things, that a certain parameter set is not necessarily suitable for simulating MOSFET–C filters if the mode of operation in which a MOSFET resistor works (linear, with a high channel-bulk voltage) was not kept in mind by the person or people who did the parameter extraction. Because only a very small number of foundry customers do at present use MOSFET resistors, one can safely assume that modelling the operation of MOSFET resistors had low priority for the modellers. We do not know this for certain, but measurements of the test structures[2] showed a mediocre quantitative agreement with the models. We also never managed to build a MOSFET–C filter that had a pole frequency in the range where it should have been according to the simulations.

Using MOSFET–C in industrial applications

If MOSFET–C filters are to be built for certain applications, it is very important to use bulk-referenced models such as the EKV model [Enz95, Bucher96b, Bucher96a], and to make sure that the parameters are suitable for modelling MOSFET resistor. If they are not, a specialised company should be hired to do the parameter extraction. Otherwise, at least one design–fabrication–re-design cycle will be necessary.

Qualitatively, simulations and measurements agree well

In spite of all these problems, a combination of measurements, simulations and calculations can still give valuable insights into MOSFET–C filters. One reason for this is that while the models do not give quantitatively exact results, they at least give results that agree qualitatively with the measurements. For example, Fig. 5.3 shows a comparison of measured and simulated harmonic distortion curves of the charge-pumped

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[1] Tutorial given by Daniel Foty from Gilgamesh Associates at the ISCAS 2000 in Geneva.

[2] These measurements were made by Dr. Władysław Grabiński.
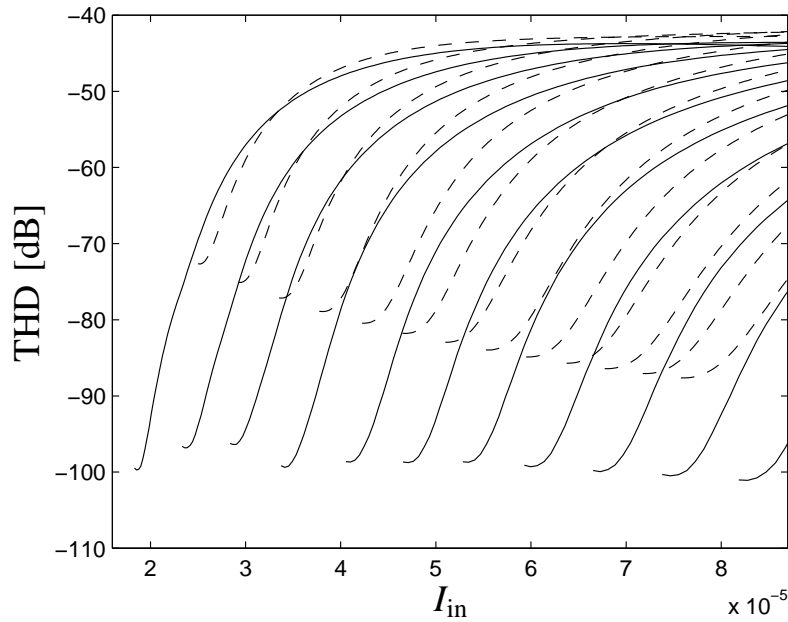
Total harmonic distortion of a charge-pumped biquad vs. input current for charge-pump supply voltages ranging from 2.7 V (left) to 3.3 V (right) in steps of 0.05 V. The solid curves are measurements, the dashed curves are simulations.

Figure 5.3

biquad discussed later in this section and in Sec. 7.4.2; other comparisons show a similarly good qualitative match.

Second-order MOSFET–C networks   5.4

The possibility of implementing single-amplifier biquadratic filters as MOSFET–C filters was already briefly mentioned in 1988 [Czarnul88], where it was also stated that the method gives too much harmonic distortion when it is applied to Sallen-and-Key filters. As explained above, [Czarnul88] neglects clipping, which plays a little role in audio-frequency, highly linear filters, but is the main source of harmonic distortion in MOSFET–C video-frequency filters. We will therefore first look at clipping-induced harmonic distortion occurring in the Sallen-and-Key filter shown in Fig. 5.4.

Sallen-and-Key
MOSFET–C filters

The harmonic distortion shown in Fig. 5.3 is mainly caused by signal clipping. The transition from regions of low distortion to regions of high distortion is comparatively steep. Therefore,

Evaluating
clipping-induced
distortion
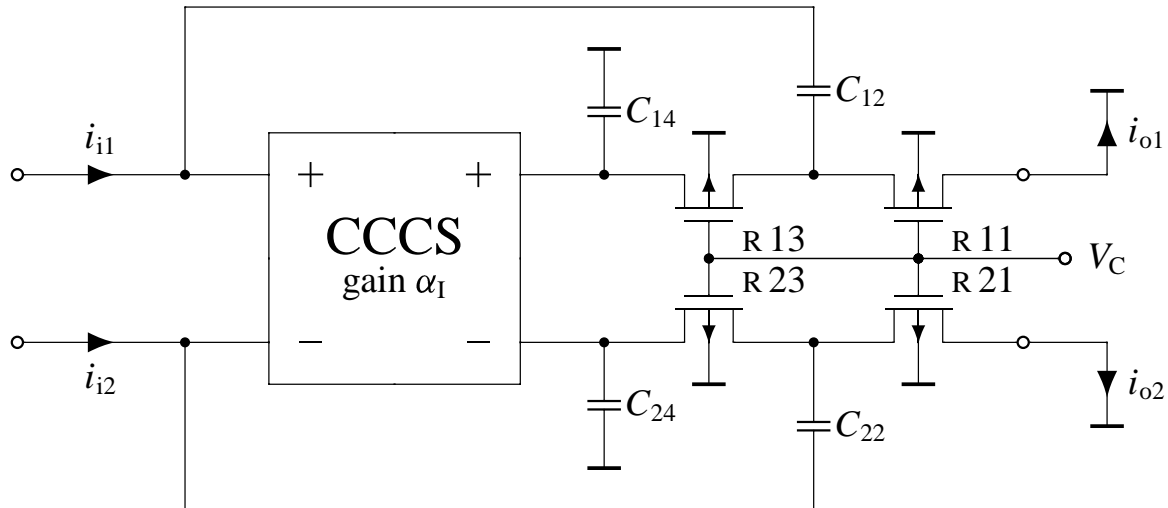
Figure 5.4   *Sallen-and-Key filter built as a MOSFET–C filter with a current amplifier (CCCS).*

	nMOS	pMOS	
V_{T0}	0.85	$-0.92^{†}/-0.85^{‡}$	[V]
$\mu \cdot C_{ox}$	120	40	[$\mu A/V^2$]
γ	0.8	0.5	[$\sqrt{V}$]
ϕ_0	0.94	0.91	[V]
$\alpha_{n,p}$	2.35	1.30	

Table 5.1   *Typical threshold voltages, transconductance parameters, body factors, characteristic potentials and noise correction factors (c.f. Sec. 6.3.2) of the AMS 0.6 μm CMOS process ([†]first chip, [‡]second chip).*

as a first approximation, one can say that the limit on the possible input current is the point where either the output transistors of the current amplifier leave the saturation region or where the MOSFET resistors leave the linear region. This has implications on where the analogue ground of the SAB should be chosen.

Choosing analogue ground

This will now be shown using the biquad described in Sec. 7.3.3 as an example. Tab. 5.1 shows the parameters of the 0.6 μm CMOS process by Austria Mikro Systeme. Note that the foundry changed the V_{T0} of the pMOS transistors from -0.92 V to -0.85 V between the fabrication of our first and second chip.

Two different effects can lead to signal clipping. First, if any terminal voltage of a MOSFET resistor goes too close to the gate, then the MOSFET saturates. Second, if the output terminal voltage of the current amplifier goes too close to either rail, then the respective cascode transistor leaves the saturation region, and the current amplifier output resistance drops. Since the clipping is similarly hard in both directions, it makes sense to choose the analogue signal ground voltage V_A in the middle between the pinch-off voltage of the MOSFET resistors and the voltage where all cascode transistors are just saturated. According to [Tsividis96], the pinch-off voltage becomes

$$(5.1) \quad V_P = \frac{V_C - V_{T0}}{m_0} \qquad \text{with} \qquad m_0 = 1 + \frac{\gamma}{2\sqrt{V_A + \phi_0}},$$

where V_C is the gate control voltage of the MOSFET resistors, and m_0 is a body effect parameter (c.f. Tab. 5.1 for the other parameters). Note that all voltages are related to the MOSFET resistor's bulk, i.e. to V_{dd} for a pMOS and to V_{ss} for an nMOS resistor.

In our design, we chose $V_A = 1.65$ V, i.e. the middle between the rails, and $V_C = 3.3$ V. Therefore $V_P = 2.06$ V for pMOS resistors and $V_P = 1.96$ V for nMOS resistors. Thus pMOS resistors are preferred, because they offer a higher voltage swing and therefore a better SFDR. The resistance of a MOSFET resistor is [Tsividis96]

$$(5.2) \qquad R_{p\text{MOS}} \approx \left(\frac{W}{L} \mu C_{\text{ox}} (V_C - V_{T0} - m_0 V_A) \right)^{-1}.$$

At low frequencies, the capacitors in Fig. 5.4 are not effective, and R 11 and R 12 act as one single pMOS resistor of size 44×4.3 μm. Thus $R_{p\text{MOS}} = 5.17$ kΩ in our example. The

maximum possible voltage swing before pinch-off occurs is

$$(5.3) \qquad\qquad V_{\max} = V_{\mathrm{P}} - V_{\mathrm{A}} ,$$

making $V_{\max} = 0.41\,\mathrm{V}$. Finally, the maximum signal current which can flow through the MOSFET resistors is the saturation current of the pMOS resistor,

$$(5.4) \qquad I_{\max} = I_{\mathrm{sat}} = \frac{W}{L}\mu C_{\mathrm{ox}}\,(V_{\mathrm{G}} - V_{\mathrm{T0}} - m_0 V_{\mathrm{A}})^2 ,$$

and therefore $I_{\max} = 91\,\mu\mathrm{A}$.

The optimum analogue ground

It can easily be seen that the choice $V_{\mathrm{A}} = 1.65\,\mathrm{V}$ is not very good, since the voltage can only swing by $V_{\max} = 0.42\,\mathrm{V}$ towards the negative rail but by a full threshold voltage $|V_{\mathrm{T0}}| = 0.92\,\mathrm{V}$ towards the positive rail, with M 63's cascode (c.f. M 3 in Fig. 5.5) still being saturated. As discussed above, V_{A} should be set between V_{P} and $V_{\min}$,

$$(5.5) \qquad\qquad V_{\mathrm{A}} = \frac{V_{\mathrm{P}} + V_{\min}}{2} .$$

If the cascodes are biased by the mid-rail voltage, $V_{\mathrm{dd}}/2$, then $V_{\min} = V_{\mathrm{dd}}/2 - |V_{\mathrm{T0}}| = 0.73\,\mathrm{V}$. Inserting (5.5) into (5.1) results in

$$(5.6) \qquad V_{\mathrm{A}} - \frac{V_{\min}}{2} = \frac{(V_{\mathrm{C}} - V_{\mathrm{T0}})\sqrt{V_{\mathrm{A}} + \phi_0}}{\gamma + 2\sqrt{V_{\mathrm{A}} + \phi_0}} ,$$

whose symbolic solution does not provide much insight. Solving it numerically for the process parameters in Table 5.1 (first chip) results in $V_{\mathrm{A}} = 1.39\,\mathrm{V}$, which is $0.26\,\mathrm{V}$ closer to V_{dd} than the local analogue ground we chose on our chip. It can be seen from (5.2) that moving the analogue ground to $V_{\mathrm{A}} = 1.39\,\mathrm{V}$ reduces the sheet resistance by a factor of 1.61. Thus, for maintaining the same resistance, the width of the MOSFET resistors must be reduced from $44\,\mu\mathrm{m}$ to $27.3\,\mu\mathrm{m}$. Then the new saturation current can be calculated as before using (5.4), resulting in $I_{\max} = 147\,\mu\mathrm{A}$. Therefore, moving the analogue ground by $0.26\,\mathrm{V}$ towards the positive rail increases the maximum allowable current by $4.2\,\mathrm{dB}$.

Why pMOS resistors are used

Note that choosing the optimum V_{A} for pMOS resistors increases the voltage margin available for operating M 11. On

the other hand, moving the analogue signal ground towards the negative rail, as would be necessary with nMOS resistors, would make M 11 almost inoperable. nMOS resistors could therefore only be used if nMOS instead of pMOS transistors were used in the voltage buffer. This is, however, not advisable in an n-well process such as the one used in this thesis, and even in a p-well process, it would mean that the actual current mirroring would have to be performed by pMOS transistors, decreasing the speed of the current amplifier.

Charge-pumped MOSFET–C filters 5.5

In a charge-pumped MOSFET–C filter, such as the one in Sec. 7.4.2, things are different, since the gate control voltage of the MOSFET resistors will normally lie far enough above the positive rail so that the MOSFET resistors never saturate (note that this time only nMOS resistors can be used, since a charge pump cannot generate voltages below V_{ss}). The maximum current at which signal clipping occurs is then determined only by the output stage of the current amplifier. In this case, the analogue ground can normally be chosen in the middle between the rails. An important question is then how large the possible voltage swing at the output of the current amplifier should be chosen in order to maximise the SFDR of the filter. Surprisingly, the result is barely technology-dependent, as we will now show.

The optimum analogue ground is mid-rail

Choosing the signal swing 5.5.1

The output transistors of our current amplifier, M 61 and M 63, are cascode transistors whose gates are connected to mid-rail (see Fig. 5.5). On the second chip, $V_{T0n} = V_{T0p} = V_{T0} = 0.85\,\text{V}$. Thus the maximum signal swing such that the signal at Z is not clipped becomes $\pm V_{T0}$. The voltage margin available to accommodate the saturation voltage V_{dsat} of both transistors in, e.g., M 63 is $V_{dd}/2 - V_{T0} = 0.8\,\text{V}$ for $V_{dd} = 3.3\,\text{V}$ and $V_{T0} = 0.85\,\text{V}$.

Signal swing limits
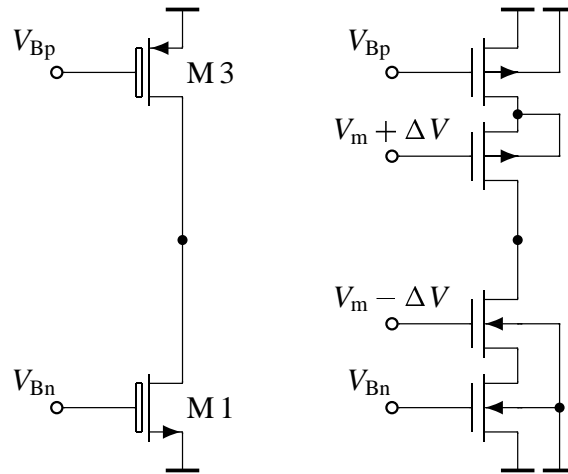
Figure 5.5   *Composite transistors used in the current amplifier.*

<div style="float:left; width:25%">

Increasing voltage
swing and noise

</div>

Moving the bias voltage closer to the rails by a voltage ΔV
increases the voltage swing to $\pm(V_{T0} + \Delta V)$ and decreases the
voltage margin within the cascodes to $V_m = V_{dd}/2 - V_{T0} - \Delta V$.
If the distribution of the voltage margin between the main
transistor and the cascode transistor remains the same, $V_{dsat\,main}$
decreases by a factor of

$$(5.7) \qquad k = \frac{V_{dd}/2 - V_{T0}}{V_{dd}/2 - V_{T0} - \Delta V} \, .$$

To achieve this, both transistors are made wider by a factor
of k^2. However, the speed of the CCCS depends on the ratio
$g_m/C_{gs} = c \cdot V_{dsat}/L^2$ of the main transistors, where c is a
design-independent quantity. To maintain the same speed, we
need to scale the length of the main transistor by $1/\sqrt{k}$ and its
drain current I_D by $\sqrt{k}$. It then follows from $g_m = 2\,I_D/V_{dsat}$
that g_m becomes $k^{3/2}$ times larger. Finally, the RMS of the
noise current is proportional to $\sqrt{g_m}$ and increases by a factor
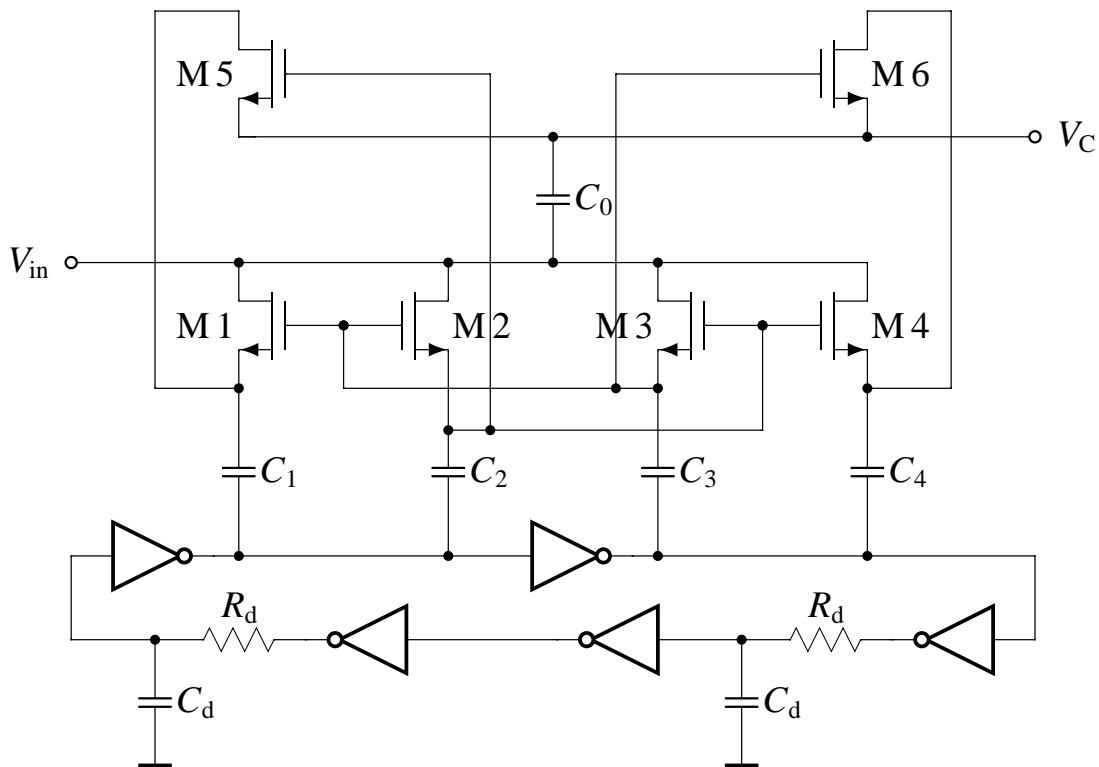of $k^{3/4}$.

Minimum SNR   This can now be compared to the increase of the voltage swing,

$$(5.8) \qquad k' = \frac{\Delta V + V_{T0}}{V_{T0}} \, .$$

The SNR is scaled by $k'/k^{3/4}$. The optimum ΔV is:

$$(5.9) \qquad \frac{d}{d\,\Delta V}\frac{k'}{k^{3/4}} = 0 \quad \Longrightarrow \quad \Delta V = \frac{2}{7}V_{dd} - V_{T0} \, .$$

Self-oscillating two-stage charge pump. (The inverters are   **Figure 5.6**
connected between V_{in} and V_{ss}.)

In our example, $\Delta V = 0.09\,\mathrm{V}$, which is not quite the bias
voltage we used in our current amplifier. However, a numerical
evaluation shows that only 0.1 dB of SNR is lost by connecting
the gates of the cascode transistors to analogue ground, which
by no means justifies using a bias voltage generator.

Finally, note that the same result is also valid if $V_{T0n} \neq V_{T0p}$.   When V_{T0} is different
It is then only necessary to replace V_{T0} in all formulae by   for nMOS and pMOS
$(V_{T0n} + V_{T0p})/2$ if the analogue ground can be chosen freely,
or to replace it by $\min\{V_{T0n}, V_{T0p}\}$ if the analogue ground must
be in the middle between the rails.

A charge pump for MOSFET–C filters   5.5.2

The charge pump shown in Fig. 5.6 combines features of the   Operation principle
one proposed by Duisters and Dijkmans in [Duisters98] with
those of a five-inverter ring oscillator. It actually comprises
two charge pumps. The main pump, consisting of M 1, M 4,
M 5, M 6, $C\,1$, and $C\,4$, fills the tank capacitor $C\,0$ with charge,

All nMOSTs	$10 \times 0.6\,\mu\text{m}$
All pMOSTs	$33 \times 0.6\,\mu\text{m}$
R_d	$4.8\,\text{k}\Omega$
C_d, C_2, C_3	$0.5\,\text{pF}$
C_1, C_4	$1\,\text{pF}$
C_0	$20.5\,\text{pF}$

Table 5.2 *Transistor dimensions and component values in the charge pump.*

where M 5 and M 6 alternatively conduct the charging current. A second pump driven by the same inverters, consisting of M 2, M 3, C 2, and C 3, sets the gate voltage of M 5 and M 6 to $2\,V_\text{in}$ while they charge C 0. Thus the output voltage becomes

$$(5.10) \qquad\qquad V_\text{C} \leq 2\,V_\text{in} - V_\text{T5}\,,$$

where M 5's threshold voltage V_T5 is comparatively large because of the bulk effect (we are using an n-well process). In our example, $V_\text{C} = 4.6\,\text{V}$ for $V_\text{in} = 3\,\text{V}$. The charge pump operates properly for $V_\text{in} = 1.3\ldots3.3\,\text{V}$, resulting in $V_\text{C} = 1.5\ldots5.3\,\text{V}$.

Voltage ripple magnitude

The voltage ripple of this charge pump is smaller than that of a conventional charge pump by a factor of $g_\text{m5}/g_\text{ds5} \approx 30\ldots100$. The voltage ripple of a single-stage charge pump is [Duisters98]

$$(5.11) \qquad\qquad V_\text{ripple} = \frac{1}{2} \cdot \frac{I_\text{out}}{C_0\,f_\text{clk}}\,,$$

where I_out is the DC current flowing out of the tank capacitance C_0 and f_clk is the pump's clock frequency. This means that if V_ripple, I_out and f_clk are the same, the two-stage charge pump needs a tank capacitor which is $30\ldots100$ times smaller than the one in a conventional charge pump. The fact that it still requires $20.5\,\text{pF}$ of capacitance for an acceptably low voltage ripple shows that one could not actually afford the chip area that a conventional charge pump would require.

Design of the ring oscillator

We designed the oscillator with an oscillation frequency that is well beyond the pole frequency of the filter, i.e. around $90\,\text{MHz}$. Since the inverters need to deliver only small currents, they can be built with small transistors. Using only inverters

would result in an oscillation frequency of almost 1 GHz, thus two passive one-pole low-pass filters, each consisting of one poly resistor and one poly-poly capacitor, had to be used to slow the oscillator down to 90 MHz. This has the additional advantage that it reduces the temperature dependence of f_{clk}. A transient simulation using worst-case process parameters and temperatures showed that the oscillation frequency can be expected to be between 70 MHz and 115 MHz, with a typical value of 93 MHz and a charge-pump output voltage ripple of 4 mV. The measured oscillation frequency was then between 62 MHz and 71 MHz for a charge-pump supply voltage going from 2.7 V to 3.3 V. This variation is uncritical, since the exact oscillation frequency is irrelevant as long as the clock feed-through is not too strong. Table 5.2 shows the transistor dimensions and component values used in the charge pump. The layout of this charge pump and further measurements will be discussed in Sec. 7.4.2.

Clock feed-through   5.5.3

The main problem with using a charge pump to generate a higher control voltage is that clock feed-through occurs. There are two paths through which the clock has an influence on the filter output current: one is via a ripple on the control voltage, and the other is through electro-magnetic coupling and through substrate noise.

Two feed-through paths

The control voltage ripple is fed through to the output by two different mechanisms. First, it leaks in through the gate capacitance of the MOSFET resistor. To keep this effect small, the clock frequency f_{clk} must be in the stop-band of the filter. For our 24-MHz low-pass biquad, we chose $f_{clk} \approx 90$ MHz. Simulations show that a voltage ripple of 5 mV causes an output current ripple of 10 nA, independent of the signal. Compared to the maximum output current for 50 dB harmonic distortion, 30 μA, this is a ripple of −70 dB, which is negligible. More important than the linear clock feed-through is that the voltage ripple *modulates* the signal. Fig. 5.7 shows the simulated spectrum at the filter output for a 2-MHz, 10 μA (at the output) signal and a 5-mV, 90-MHz control voltage ripple. It can be seen that mixing products appear at 88 MHz and at 92 MHz.

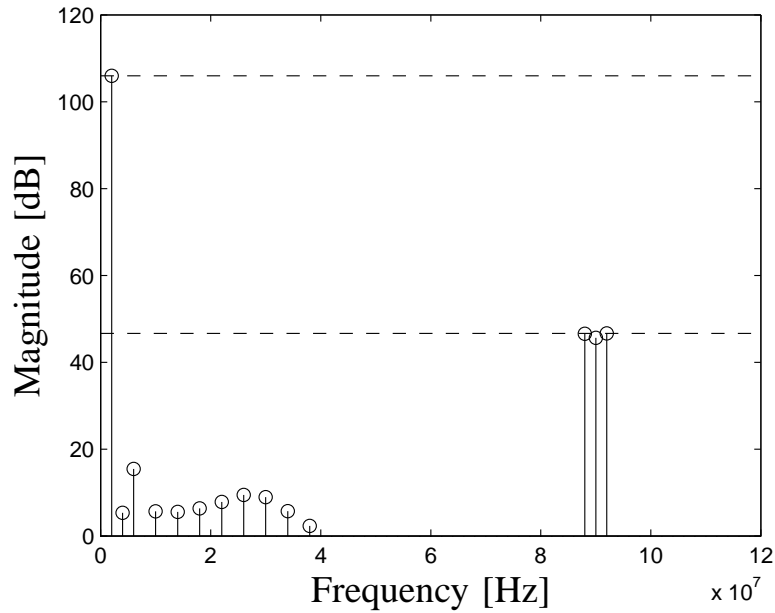*Linear feed-through and mixing effects*

Figure 5.7   *Output current spectrum (0 dB denote 0.5 nA).*

Their magnitude is proportional to the input signal magnitude. Simulations showed that both peaks lie 58 dB below the signal, giving a total distortion of −55 dB.

Substrate-noise measurements

Figure 5.8 shows the measured output spectrum of the charge-pumped filter for $V_{in} = 3.3$ V and a strong input signal at five different frequencies. The spectra have been scaled such that they can be shown in one coordinate system. The mixing products are clearly visible, but they are considerably weaker than the feed-through of the oscillation frequency. This excess feed-through is, however, not caused by the filter, but by a *very* bad layout mistake. The output lines of the filter are drawn on the metal-3 layer on top of the guard ring around the charge pump (see Fig. 5.10). One output line follows the guard bar for a length of 100 μm, and both follow the supply rail of the charge pump straight to the pads. One problem is that this kind of clock feed-through cannot easily be simulated, but it can be clearly seen in Fig. 5.9, which shows three spectra (note that the frequencies of (a) and (c) are shifted by +5 MHz and −5 MHz to make the peaks visible). Curve (a) shows the charge-pumped biquad that is driven by a strong 2-MHz input signal. Curve (b) is the same with the biquad switched off. The two peaks around 70 MHz have almost the same height, but the difference is probably due to the different input range of the spectrum analyser. Thus, only a very small part of the clock
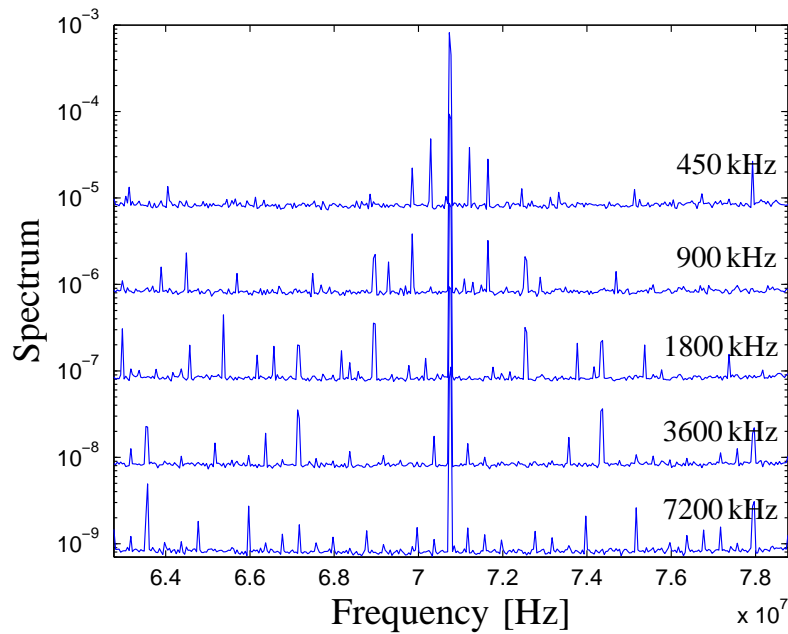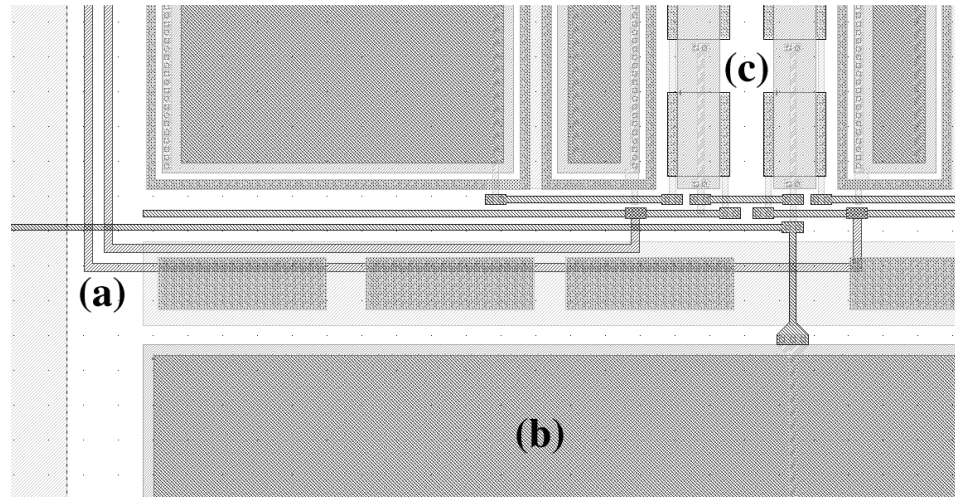
Measurement of the clock feed-through (the Spectrum units are arbitrary, see text).   **Figure 5.8**
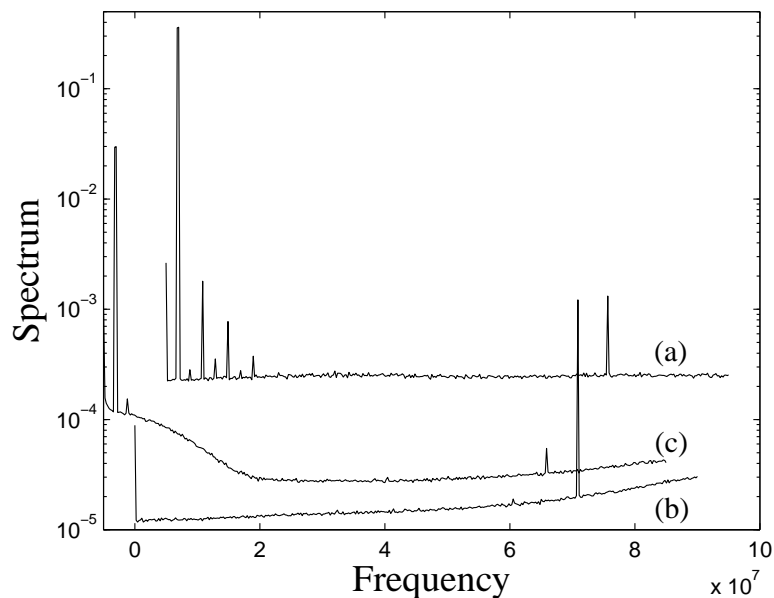
Clock feed-through at the biquad output pins (a), when the biquad is switched off (b), and in the 7th-order filter (c) described in Sec. 7.4.3.   **Figure 5.9**

Figure 5.10   *Layout of the charge pump and filter. (a) output signal lines; (b) charge pump capacitor; (c) MOSFET–C network.*

feed-through goes through the filter. This view is supported by curve (c), which shows a similar measurement (same charge-pump, different input signal) with the 7th-order filter described in Sec. 7.4.3. The clock fed through to the output of this filter is about 26 dB weaker.

MOSFET–C SABs reject substrate noise well

Thus we can conclude that MOSFET–C SABs reject substrate noise well, certainly well enough for most applications; the power of the clock signal fed through to the output of the 7th-order filter is smaller than the noise power and scarcely changes the SNR of the filter.

5.6   Various influences on the THD

Using faster simulation and measurement methods

Conventionally, the THD of a biquadratic low-pass filter is measured at one fifth of the pole frequency. This is done such that the harmonics up to the fifth are still in the pass-band of the filter. Simulating harmonic distortion is, however, much faster using DC sweeps than transient analyses, and measuring harmonic distortion is much faster using the power sweep mode of a network analyser than using a spectrum analyser. We will illustrate this now with some measurements and then discuss it in more detail in Sec. 5.8.
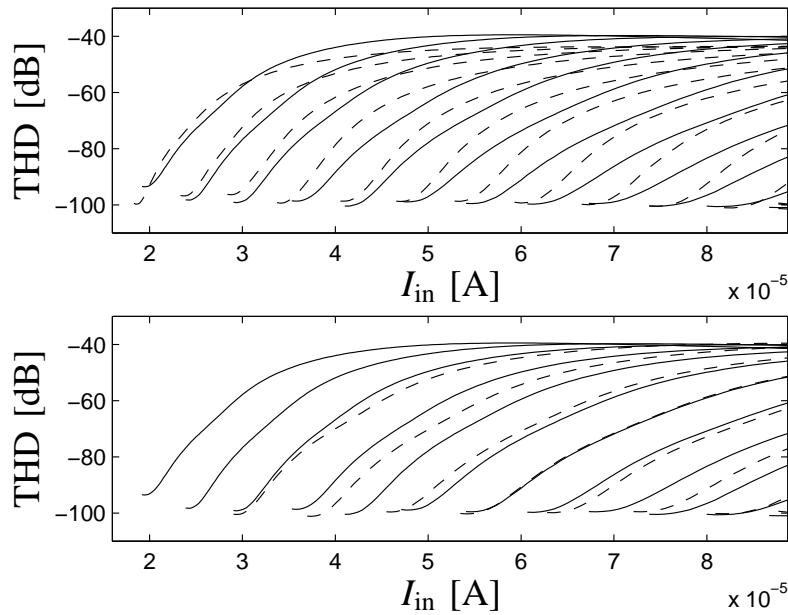
THD for $V_{in} = 2.7 \ldots 3.2\,V$ (left to right), corresponding to $V_C = 3.9 \ldots 4.8\,V$. Top: Measured at $f_p/5$ (solid) and at 100 kHz (dashed). Bottom: Measured at $f_p/5$ (solid) and at f_p (dashed).

Figure 5.11

Frequency dependence of the THD   5.6.1

Fig. 5.11 shows harmonic distortion measurements for different charge-pump supply voltages (and therefore gate control voltages) with signals at 100 kHz, $f_p/5$ and f_p (these values differ for different control voltages). It can be seen that the harmonic distortion is qualitatively and quantitatively very similar at 100 kHz and at $f_p/5$, thus the DC-characteristic simulation method and the power-sweep measurement method described in Sec. 5.8 can well be used for gaining insight into MOSFET–C filters. Note that harmonic distortion is much lower at f_p, because then the third harmonic lies in the stop-band and is damped by the filter, whereas the signal is q_p times stronger than at low frequencies.

Clipping distortion scarcely depends on the signal frequency

Mismatch-induced distortion   5.6.2

Figure 5.12 shows the rising edges of the THD curves for a mismatch-free filter and for twelve Monte-Carlo runs sim-ulating component mismatch. The BSIM 3v3 Monte-Carlo

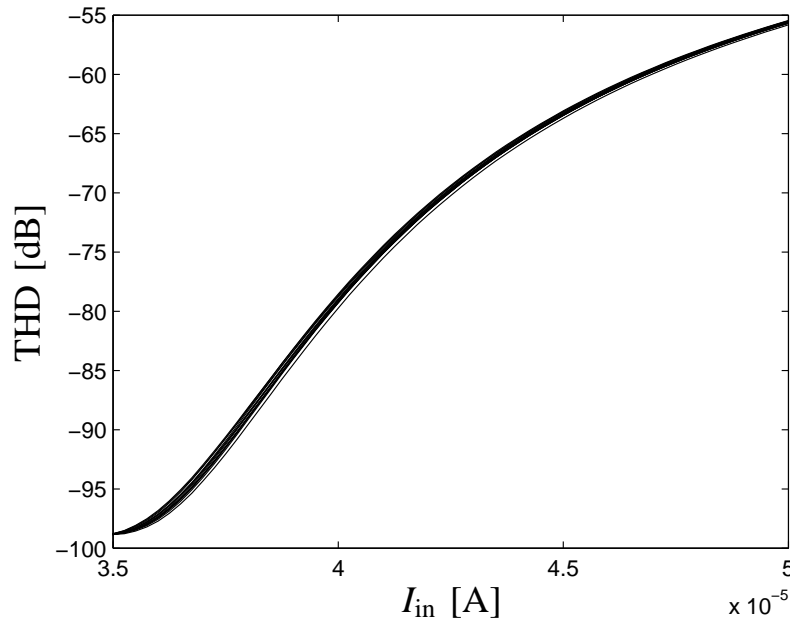*Mismatch-induced distortion plays a minor role*

Figure 5.12   *Simulated THD, one mismatch-free filter and twelve*
Monte-Carlo runs simulating mismatch.

models supplied by AMS were used for these simulations, and
the gate control voltage was set to 4.6 V. The curve of the
mismatch-free filter lies in between the other curves, but all
curves are close together. It is apparent that mismatch-induced
distortion plays a minor role. There are two reasons for this.
First, the main limit on the maximum possible input current
is set through the points where some transistors saturate or
others leave the linear region. These points mainly depend on
process variations; matching is not really an issue. Second, all
transistors in the current amplifier are comparatively large, thus
the two signal paths in the filter will match well. In low-voltage
video-frequency filters, the transistors will generally have to be
large, so mismatch will not be a problem with video-frequency
MOSFET–C SABs.

5.6.3   Distortion caused by cascading biquads

Clipping caused by
the second biquad

The above simulations were all made with ideally loaded
filters. The situation is a little different when a biquad is
loaded by another biquad that has a higher input resistance. To
compensate for the comparatively high input impedance of the
next stage, the resistances of the MOSFET resistors $R\,11$ and
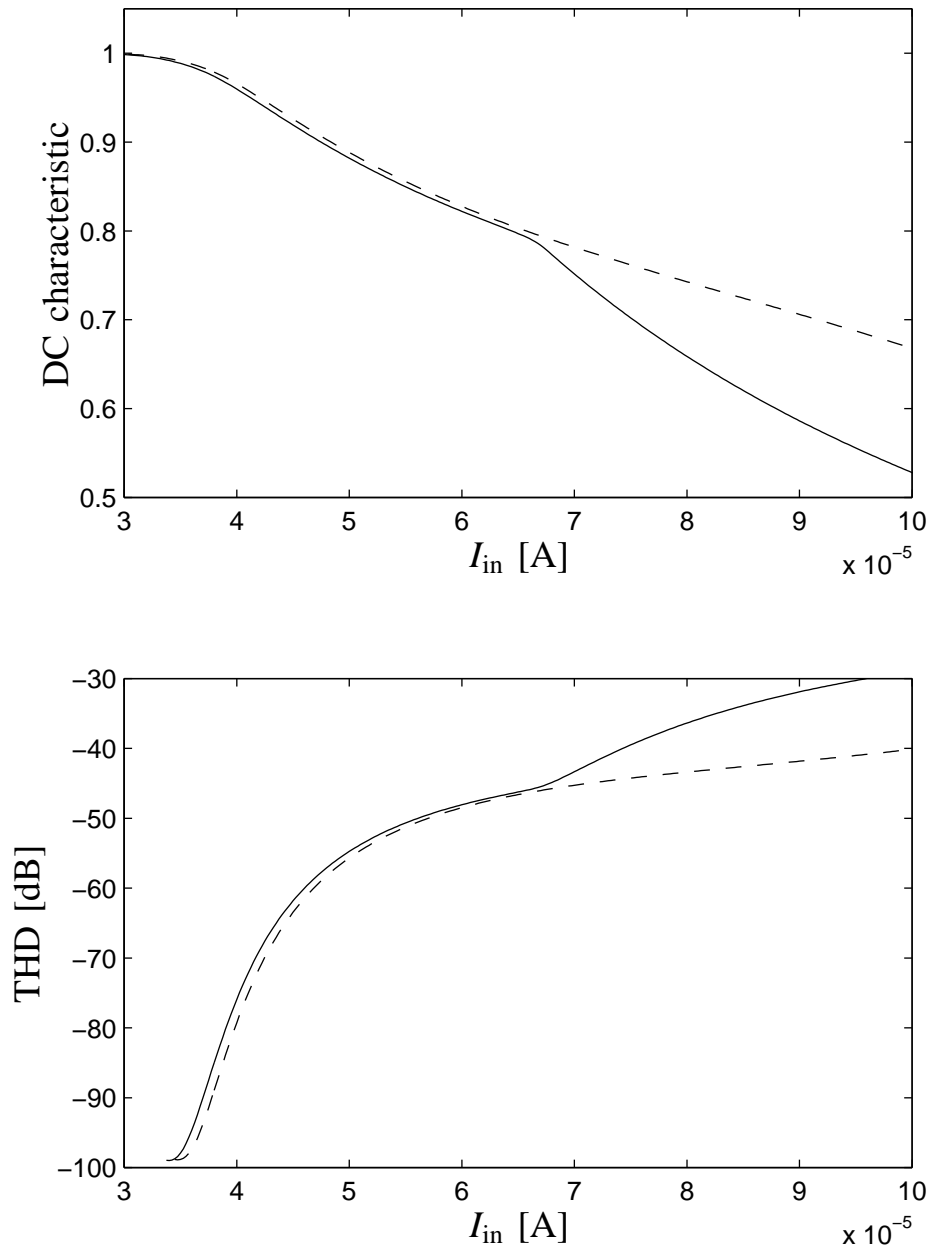
Normalised DC characteristic and simulated THD for ideal load (dashed) and loaded by another biquad (solid).

Figure 5.13
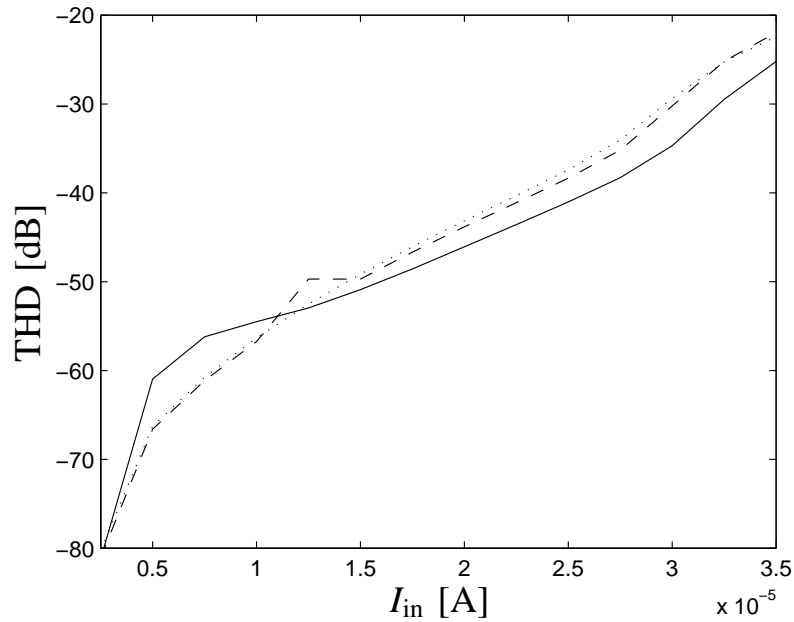
Figure 5.14   *Simulated THD of the original MOSFET–C SAB (solid), a MOSFET–C SAB without a C14 and C24 (dashed), and a MOSFET–C SAB with enlarged C14 and C24 (dotted).*

R 21 must be decreased; in the case at hand their width was increased from 12 μm to 14 μm. Figure 5.13 shows both the DC characteristics and the THD curves of the ideally loaded biquad (dashed) and the biquad loaded by another current amplifier. The maximum allowable current is scarcely decreased in this example, but it is apparent that, at a certain input current ($\approx 65\,\mu A$), the input of the second current amplifier saturates and introduces hard clipping. As long as this hard-clipping point is above the maximum input current supported by the first stage, cascading biquads has little influence on the THD produced by one stage. It follows that the gain of one biquad should be as low as possible in order to make the cascading of the biquads easier.

5.6.4   Distortion caused by amplifier output capacitance

The non-linearity of the amplifier output capacitance plays a minor role

Some harmonic distortion is also caused by the non-linear nature of the current amplifier's output capacitance. To illustrate this, Fig. 5.15 shows the THD of the original charge-pumped biquad (solid), the THD of the same circuit with C 14
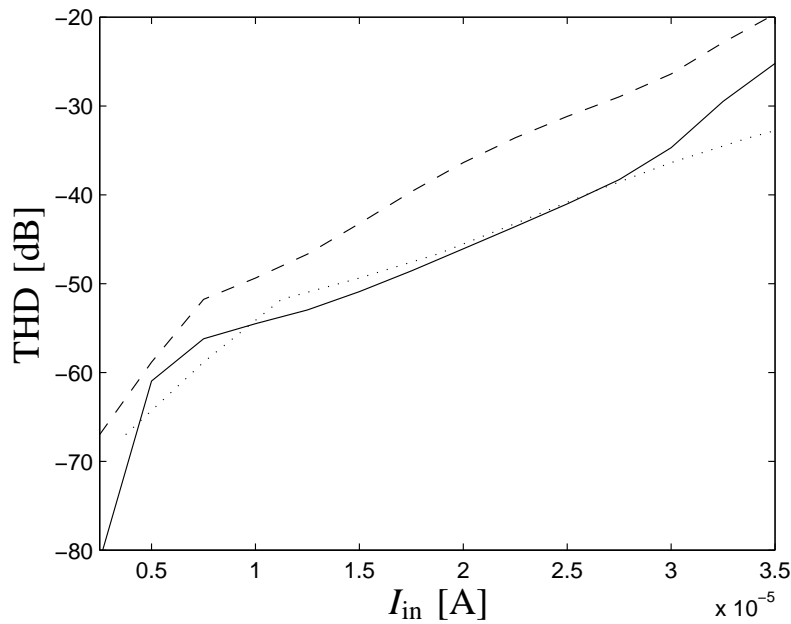
Simulated THD of a conventional MOSFET–C SAB (solid),
of a MOSFET-only SAB (dashed),
and the latter with I_{in} scaled by 1.5 (dotted).

Figure 5.15

and C 24 removed (c.f. Fig. 5.4) and the cascode transistors at
the current amplifier output made wider by 75 % such that f_p
and q_p of the filter remain the same (dashed), and the THD with
C 14 and C 24 enlarged by 80 % and the cascode transistors
shrunk to 25 % of their original width. Note that the latter
possibility is not really feasible; in order to keep the main
transistors saturated in the simulation, ideal voltage sources
providing a negative voltage offset had to be introduced
between the main transistors and the cascode transistors.
Nevertheless, it appears that there is little difference in the
harmonic distortion behaviour of the three filters.

MOSFET-only filters   5.7

All the poly-poly capacitors in a MOSFET–C SAB can be
replaced by pMOS gate capacitors. The resulting filter is then
compatible with standard digital CMOS processes, since only
one poly-silicon layer is needed. The balanced form of the filter
also compensates part of the non-linearity of the non-linear
gate capacitors. Fig. 5.15 shows the simulated THD of the

The SNR of
MOSFET-only is
4 dB lower

charge-pumped biquad and of the same filter with MOSFETs connected as gate capacitors instead of poly-poly capacitors. The capacitor block becomes only slightly larger (by about 25 %). The maximum possible input current is reduced to 65 % by the conversion to a MOSFET-only filter, which is a loss of only 4 dB. Therefore, single-amplifier biquadratic filters can also be used on standard digital processes with only small performance losses.

## 5.8　　Simulation and measurement of harmonic distortion

Conventional distortion simulations are very time-consuming

The main problem with the simulation and the measurement of harmonic distortion is that both are tedious and time consuming, the simulation even more than the measurements. The normal procedure to simulate harmonic distortion is the *transient method*, which is to feed a signal with one frequency component and one magnitude into the circuit and then make a spectrum analysis of the output. Thus, one transient simulation that runs long enough for the circuit to reach its periodic state is needed for *every* frequency-magnitude pair of interest. The long simulation times make it virtually impossible to use the transient method as an optimisation tool. In this section, we will first discuss three different ways of simulating harmonic distortion and then show how these alternative ways can also be used for measurements.

5.8.1　　Harmonic distortion derived from DC characteristics

Graphical approach: DC–DFT method

Figure 5.16 shows an input signal that is fed through a system with a non-linear transfer characteristic ($y = e^x$ in this case) and thus becomes harmonically distorted. One way to use this view for simulating the harmonic distortion of a circuit is very straightforward: First, use a circuit simulator (e.g., Spectre) to derive the DC transfer characteristic of the circuit in question. Then use a mathematical tool (e.g., Matlab) to make the mapping shown in Fig. 5.16 for signals of different
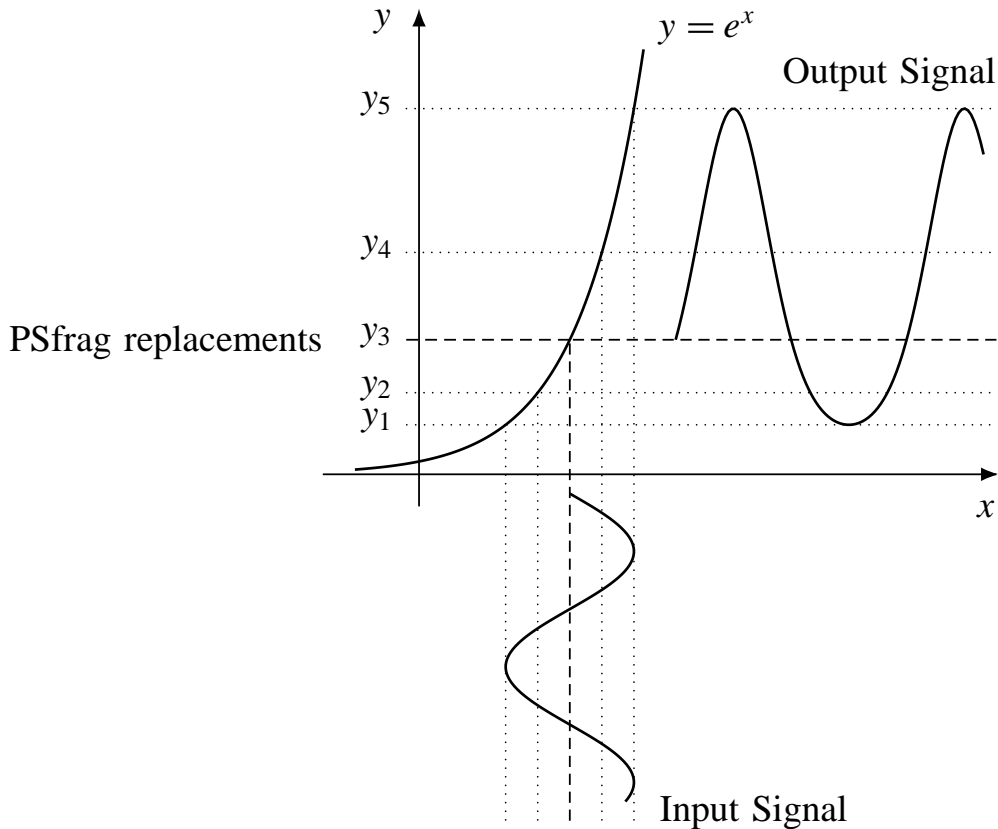
Distortion of a signal by a non-linear transfer characteristic.   **Figure 5.16**

magnitudes and calculate the harmonic distortion by doing a discrete Fourier transform (DFT, e.g. implemented as a fast Fourier transform, FFT) for one period.

We have used this method for several of the simulations in the previous sections. It has the advantage that the influence of a circuit-parameter change can be simulated very quickly, but it has the disadvantage that the frequency dependence of the harmonic distortion gets lost. For these reasons, we had to use the transient method to get the curves in Figs. 5.14 and 5.15. We have pointed out, and will demonstrated it again in Sec. 5.8.2, that this *DC–DFT method* is well suited to obtain qualitative results, although it does not necessarily predict the absolute value of the THD correctly. One disadvantage of this method is still that data has to be transferred between two independent computer tools. This makes, for example, Monte-Carlo analysis quite tedious.

Discussion of the DC-DFT method

If one is only interested in the harmonic distortion at a few magnitude points, *Espley's method* can be used, which we named after D. C. Espley who introduced it in 1933 as a

Espley: polynomial approximation

method to calculate second-order and higher-order harmonic distortion from transfer characteristics plotted in data sheets. Several methods to do this were used in Espley's time, but his method has the advantage that it works with an odd number n of *equidistant* points on the DC characteristic. For example, if $n = 3$, then the points y_5, y_3, and y_1 in Fig. 5.16 are used. Espley showed that the second-order distortion then becomes

$$(5.12) \qquad H_2 \approx -\frac{y_5 - 2y_3 + y_1}{2(y_5 - y_1)} \; .$$

He described Eq. (5.12) as a "well-known expression" in [Espley33]. However, since only H_2 can be expressed with $n = 3$, Espley extended this idea for odd $n \leq 7$. In order to calculate H_3, using $n = 5$ equidistant points is sufficient:

$$H_2 \approx -\frac{3}{4}\frac{y_5 - 2y_3 + y_1}{y_5 + y_4 - y_2 - y_1} \; ,$$

$$(5.13) \qquad H_3 \approx -\frac{1}{2}\frac{y_5 - 2y_4 + 2y_2 - y_1}{y_5 + y_4 - y_2 - y_1} \; .$$

H_4 could be calculated as well, but it is normally not relevant.

Using Espley in IC-design tools

The great advantage of Espley's method is that these rational expressions can be evaluated by the circuit simulator itself. For example, using Cadence IC design tools and the Spectre circuit simulator, the expressions for H_2 and H_3 can be programmed for different signal magnitudes as output values, and then a Monte-Carlo simulation can be evaluated directly using the Monte-Carlo data analysis tools built into Cadence. The disadvantage of this method is, however, that it gives only H_2 and H_3 at several individual signal magnitudes. The DC–DFT method, on the other hand, gives the total harmonic distortion for so large a number of input magnitudes as to make the resulting curves look continuous. So we used Espley's method only in the design process (i.e., for "playing" with parameters), but the DC–DFT method to generate the plots shown in this thesis.

Using Espley for symbolic calculations

Interestingly, Espley's method has another huge advantage: it can also be used for *symbolic* calculations, as it has recently been done in [Bruun98, Bruun99] to determine analytical expressions for mismatch-induced harmonic distortion in current mirrors.

Comparison of the methods   5.8.2

In this section, we compare the results obtained by the different simulation methods with measurements, and we also examine the simplest of symbolic methods, the calculation of Taylor series coefficients, which is the most widely used symbolic distortion analysis method because of its mathematical simplicity. The Taylor method is to do a Taylor series expansion of the DC transfer characteristic $y = f(x)$ around the operating point [Sansen99], which can always be shifted to the origin by a linear coordinate transformation. If the operating point is at $x = 0$,

Taylor approximation

$$(5.14) \quad y = a_0 + a_1 x + a_2 x^2 + \ldots, \quad a_n = \frac{1}{n!} \frac{d^n}{dx^n} f(x) \Big|_{x=0}.$$

Substituting a harmonic input signal $x = X \cos(\omega t)$ into (5.14) results in a series in terms of $\cos^n(\omega t)$. This must be transformed into a series in terms of $\cos(k \omega t)$, since the kth-order harmonic distortion H_k is defined as the ratio of the coefficient of $\cos(k \omega t)$ and the coefficient of $\cos(\omega t)$. This transformation is not trivial; if k is odd (even), every odd-(even-)order term $\cos^n(\omega t)$ with $n \geq k$ contributes to the coefficient of $\cos(k \omega t)$. To avoid the resulting infinite sums, it is normally assumed that the signals are sufficiently small such that all contributions but the one made by $\cos^n(\omega t)$ with $n = k$ can actually be neglected. This leads to the well-known formulae for the second- and third-order harmonic distortion [Sansen99]:

$$(5.15) \qquad H_2 \approx \frac{1}{2} \frac{a_2}{a_1} X, \qquad H_3 \approx \frac{1}{4} \frac{a_3}{a_1} X^2.$$

In many cases, the Taylor method is too inaccurate because of two main problems. First, the assumption made above is only valid for sufficiently small signals. On the one hand, there is no way of telling what "sufficiently small" means, short of comparing the Taylor analysis results to the results obtained through a different, more accurate method. On the other hand, many video-frequency circuits are operated with input signal magnitudes which are definitely not sufficiently small anymore. Second, the Taylor method is strictly local, it can only include

Discussion of the Taylor approximation

effects which are present at the operating point (OP), but not effects that only set on if the input signal moves away from the OP, such as, e.g., clipping or other types of hard distortion [Sansen99].

Comparison for $y = e^x$

Figure 5.17 shows H_2 and H_3 for the DC characteristic $y = e^x$, which describes an ideal bipolar transistor. Espley's method with $n = 5$ and the DFT method give very similar results even for very high distortion levels, while Espley's method with $n = 3$ and the Taylor method are similarly far off the mark. It can be shown that the results are even better for the ideal MOSFET transfer characteristic, $y = \ln^2(1 + e^x)$.

Comparison for ideal clipping

Ideal clipping is illustrated in Fig. 5.18. The inlay shows the transfer characteristic (the dashed lines indicate the operating point), and the main graph shows H_2 and H_3 calculated using the DFT method and Espley's method with $n = 5$. On the Espley curve, nothing happens until y_5 is clipped, and then both H_2 and H_3 increase rapidly. Note that a discontinuity is visible on the H_3 curve at the input magnitude 300, which is where y_4 saturates as well. As discussed above, it becomes apparent from (5.14) that the Taylor method fails. Because $a_n = 0$ for all $n = 0 \ldots \infty$, it is predicting no distortion at all.

Comparison for a random characteristic

To demonstrate how well Espley's method performs even in extreme cases, Fig. 5.19 shows the same as Fig. 5.18 for a DC characteristic consisting of random steps, generated in Matlab using `y = full(cumsum(sprand(1001,1,0.1)))`.

Comparison with measurements

Figure 5.20 presents the harmonic distortion of the current amplifier with adjustable gain from [Schmid99a] (c.f. Sec. 7.3.4), whose distortion is comparatively soft. Note that the Espley and DFT curves agree very well with measurements made using low-frequency (50-kHz) signals. The curve obtained through transient simulations has been omitted, since it just coincides with the other curves. As last example, illustrating hard distortion, Fig. 5.21 shows the harmonic distortion of the MOSFET–C filter from [Schmid99b] (c.f. Sec. 7.3.3). Here DFT and Espley disagree slightly, because, as in Fig. 5.18, the Espley curve shows a kink which is not really there. Nevertheless, both curves agree very well with transient simulations made for a few input signal magnitudes using low-frequency (50-kHz) signals (marked by $\times$). The measured curve (marked by $\circ$) disagrees considerably with the other curves in this case.
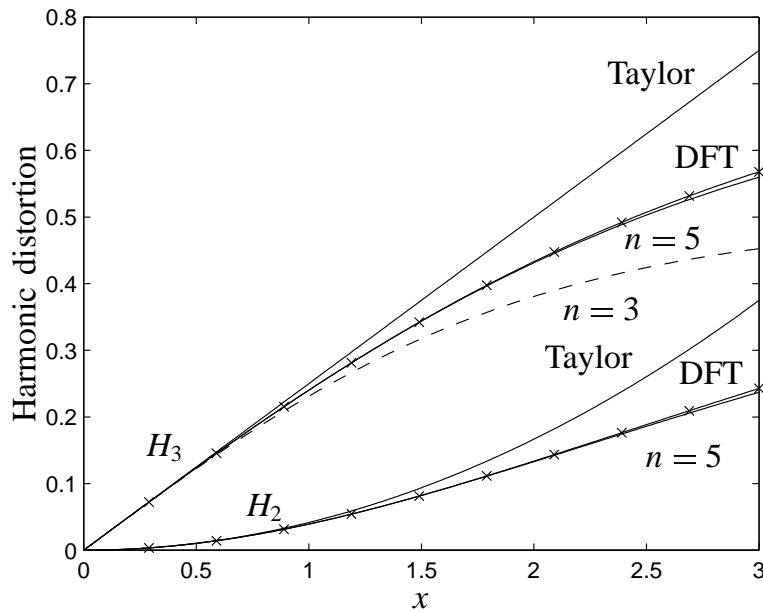
H_2 and H_3 caused by the exponential DC characteristic from Fig. 5.16.

Figure 5.17

This does not matter for our discussion, however, since the disagreement is caused by effects which are not modelled properly by the particular BSIM 3v3 transistor model we used. The same error therefore occurs for *any possible* method based on simulated data.

Measurement method

5.8.3

Finally, a transfer-characteristic-based method can also be used to make harmonic distortion measurements. Then the transfer characteristic is measured using the power-sweep function of the network analyser, and processed in a mathematical tool as if it was a DC characteristic. We used this method for some of the measurements provided in the previous sections. The advantage of this measurement method is that it is fast and gives a very good resolution in terms of signal magnitudes. In contrast to the DC–DFT simulation method, it also covers frequency-dependent influences on distortion.

Power sweep measurements

Its main disadvantage is that power-sweep characteristics are necessarily symmetrical, thus only odd-order harmonic distortion can be measured. Nevertheless, if it is first shown

Disadvantages
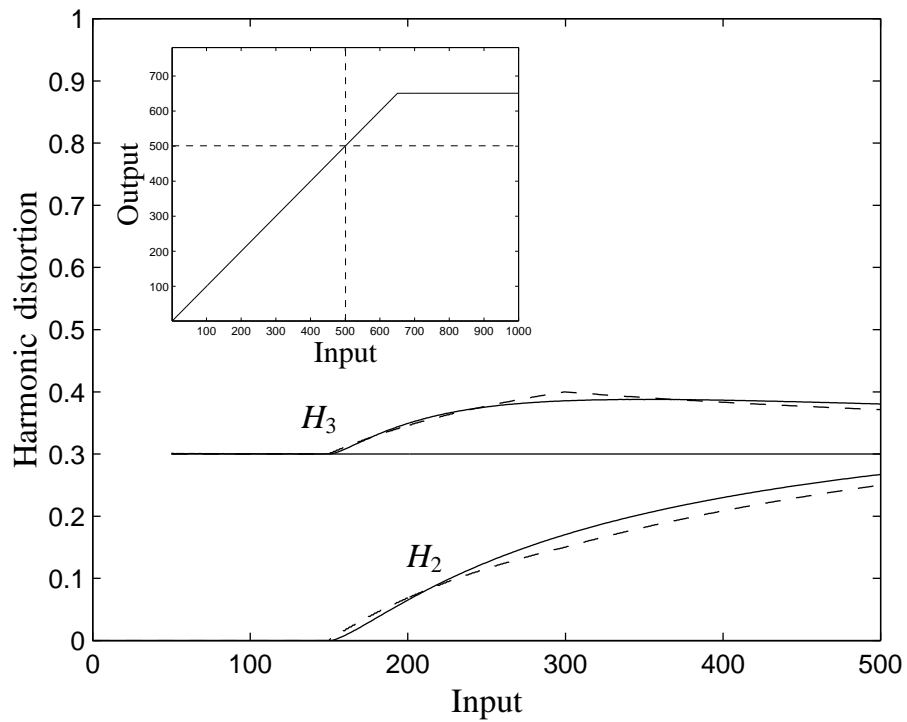
Figure 5.18   *Linear DC characteristic with clipping. Solid: DFT;*
dashed: Espley with n = 5). (Note that the H_3 curve is set
off vertically to make the figure readable.)
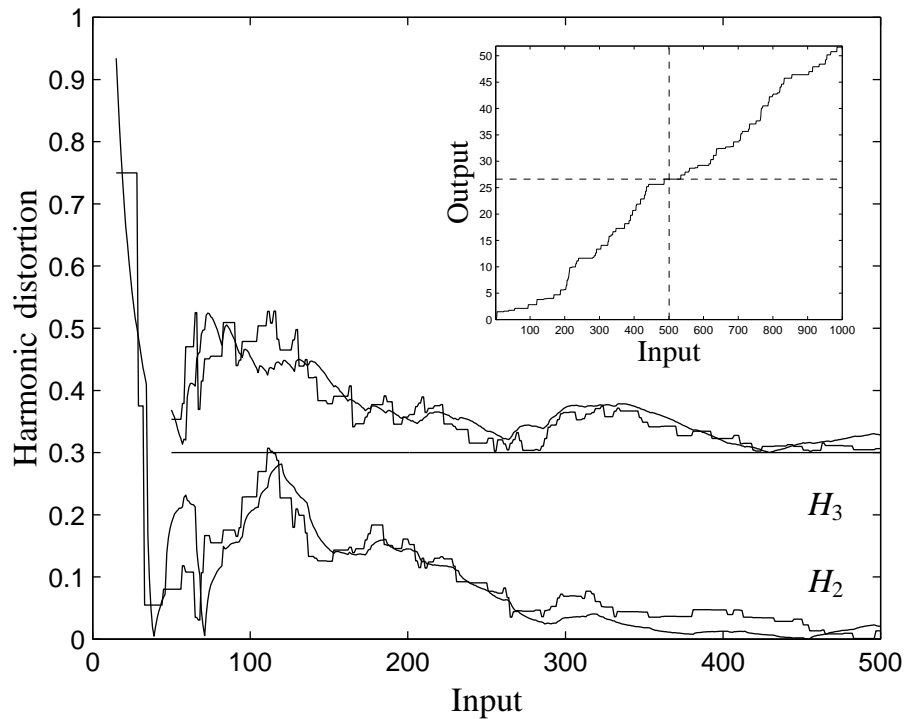
Figure 5.19   *DC characteristic consisting of random steps. Smooth:*
DFT; jagged: Espley with n = 5.
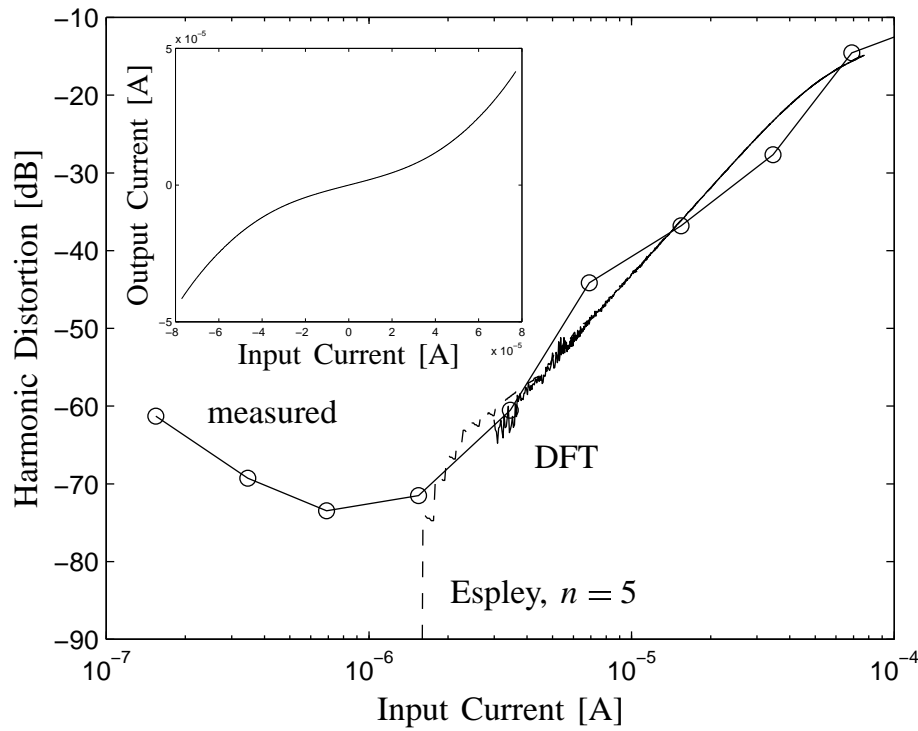
Adjustable current-controlled current source from [Schmid99a].

Figure 5.20
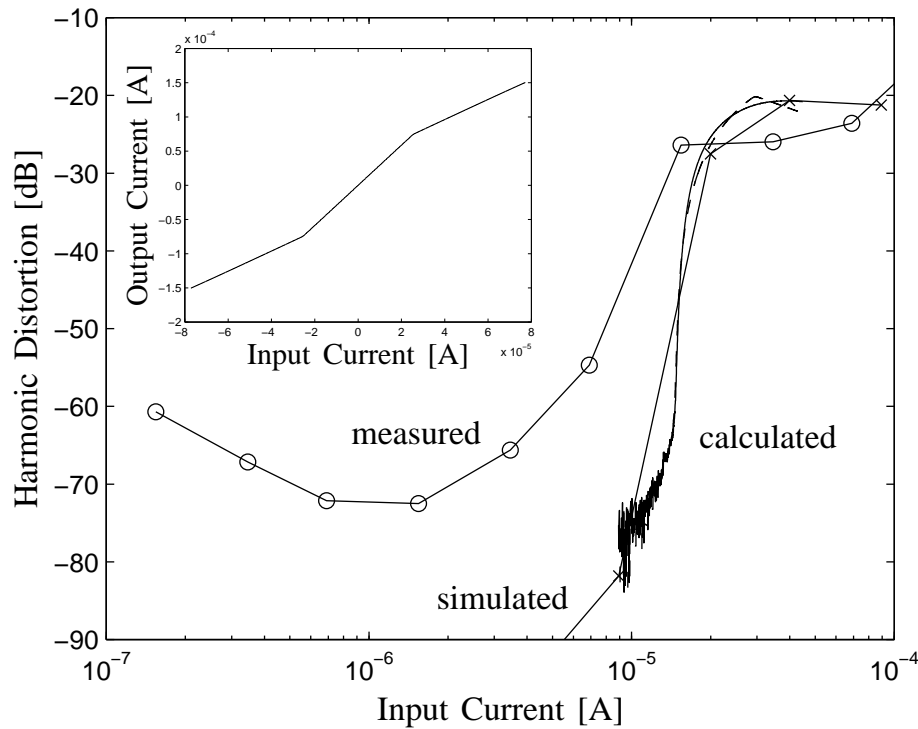
MOSFET–C filter from [Schmid99b]. Calculated curves: Espley with n = 5 (dashed) and DFT (solid).

Figure 5.21

through other methods that the main contribution to the total harmonic distortion (THD) is of odd order, then this method is a viable alternative to the much more time consuming method of using a spectrum analyser to measure the THD individually for every magnitude-frequency pair.

5.9   Conclusion

MOSFET–C SABs work

The discussion in this Chapter, together with the measurements provided in Chapter 7, show that MOSFET–C single-amplifier biquadratic filters work and are indeed a viable alternative to classical Gm–C filters. Three important questions remain open.

Suitability for mixed-signal integration

The filters we tested reject the substrate noise generated by the charge pump very well. This fact and the perfectly symmetrical structure of the filter gives rise to the assumption that they are well suited for use on mixed-signal circuits. It has yet to be shown that this is indeed the case by using our technique to integrate a true mixed-signal chip.

MOSFET–only filters

It was also shown above, by providing simulation results, that our technique can also be used to build MOSFET-only filters using a standard digital CMOS process (i.e., with one poly-silicon layer only). This possibility requires further investigations, since the THD will possibly have to be optimised using different criteria than the ones discussed in this chapter. It is also an open question whether nMOS or pMOS capacitors should be used, and if the latter are used, how the well should be polarised.

Higher-order MOSFET–C filters

Finally, it is also possible to build single-amplifier filters that generate three or more poles [Moschytz99a, Moschytz99b]. We think that this is feasible too and makes it possible to build even smaller filters with lower power consumption. However, the advance from Gm–C filters to MOSFET–C SABs is certainly much larger than the advance from MOSFET–C SABs to higher-order MOSFET–C single-amplifier filters.

Chapter 6

Implementation of the current amplifier

*It is not likely that **MAD** circuit designers will be replaced by design tools in the foreseeable future.*

(Yannis Tsividis)

This chapter is mostly descriptive, since the amplifier presented here is based on well-known concepts taken from the literature that were used to build symmetrical, balanced current amplifiers. Both the fixed-gain current amplifier and the variable-gain current amplifier presented in this Chapter can also be seen and used as second-generation current conveyors (CCIIs), as discussed in Chapter 2. Apart from a description of the amplifiers, this Chapter also discusses a few design criteria, and finally suggests improvements of the variable-gain current amplifier.

6.1   Background

What I did to build my current amplifiers and V–I converters was to take the ideas of others and convert them to a balanced, completely symmetrical form. I actually began with simulating class-AB circuits, mainly because I liked the symmetry of these circuits, but I soon started to use class-A circuits because I wanted to build 3.3-V circuits using a process with comparatively high threshold voltages. The amplifiers shown in this paper resulted from my striving for perfect symmetry and minimum complexity. I also played around with local feedback to decrease the current-input resistance and to increase the current-output impedance, but gave both up too because neither gives great advantages when one tries to push the operating frequency of an amplifier with a certain power consumption to its limits.

6.2   Current amplifier structures

Why we use CCIIs as current amplifiers

As we explained in Sec. 3.4.2, low-gain amplifiers can either be implemented as high-gain amplifiers with resistive feedback or as transistor circuits that provide the low gain without external feedback. For the reasons given in Sec. 3.4.2, we decided to use the latter implementation. As described in Chap. 2, such low-gain amplifiers are basically the same as second-generation current conveyors with arbitrary gain, or CCIIα_Is. Some possibilities to build CCIIs in CMOS were already mentioned in Chap. 2. We will now give a very brief overview of other implementations that can be found in the literature and, especially, in [Toumazou90].

Voltage level shifters in CCIIs

Most CCIIs consist of a voltage buffer whose output current is sensed, amplified and conveyed to a current output. Using a single transistor as a voltage follower is normally not sufficient, because then a voltage level shift between the Y and X terminals will occur. Thus it is necessary to place voltage level shifters (diode-connected transistors) either at the Y input or at the X input. The main disadvantage of a CCII with Y input level shifter is its non-zero offset current at the Y input. This

does not matter, however, if the CCII is to be used as a current amplifier, since then the Y input is only used to set the analogue ground at the X input (current input). A CCII with X input level shifter has no Y input offset current, but it has a higher resistance at the X input [Lidgey94, Chap. 11.5]. The CCIIs presented in Sec. 6.3 all have Y input level shifters.

A further possibility is to accurately set the X input voltage by using a voltage buffer that consists of an opamp with direct negative feedback [Sedra90, Wilson92, Wilson90]. Then the X input impedance becomes very low for low frequencies and inductive up to about the unity-gain frequency of the opamp. Then, however, the discussion about feedback vs. open loop made in Sec. 3.4.2 applies to the input stage as well. For this reason, the current amplifier presented in Sec. 6.3 does not employ local feedback. It is notable, however, that using local feedback can also give new functionality, c.f. the voltage-inverting current conveyors discussed in Chap. 2.

Local feedback

Finally, another idea is to build high-performance current conveyors by connecting several very simple current conveyors [Arbel97], just as a high-performance OTA has been built using very simple OTAs in [Nauta92].

Using simple building blocks

In the following two sections, we will present a fixed-gain current amplifier and a variable-gain current amplifier. The structures presented were mainly chosen for maximum speed and minimum chip size. Since they are to be used in MOSFET–C filters, they were also designed to be perfectly symmetrical, since any asymmetry between the two signal paths would introduce even-order harmonic distortion at the filter output (c.f. Chap. 5).

Overview

Fixed-gain current amplifier   6.3

The fixed-gain current amplifier described in this section is based on the same idea as the CCII shown in Fig. 2.10 on p. 28. The two main differences are that it is balanced and perfectly symmetrical instead of single-ended, and that it is built as a class-A circuit instead of a class-AB circuit in order to reduce the necessary supply voltage.

Balanced class-A CCII

6.3.1   Operation principle

Current subtraction   A completely symmetrical current amplifier must consist of two identical half-circuits, as shown in Figs. 6.1 and 6.2. Ideally, it is described by

$$(6.1)\qquad i_{o1} = \alpha_I (i_{i1} - i_{i2}) \qquad i_{o2} = -\alpha_I (i_{i1} - i_{i2}) \ .$$

The half circuit consists of one voltage buffer and several current mirrors. $M[1\text{–}6]3$ and $M\,11$ are constant current sources,[1] while $M[2\text{–}6]1$ form current mirrors. $M\,22$ is the input transistor. It provides, at its source, a current input with input resistance $R_{in} \approx 1/g_{m22}$. $M\,12$ is the Y-input voltage level shifter mentioned above which sets the operating point voltage of node X to V_A. Any current flowing into X is mirrored from $M\,21$ to $M\,31$ and from $M\,41$ to $M\,51$ and flows out of Z; it is also mirrored from $M\,21$ to $M\,61$ of the other half-circuit, where it flows into Z. Thus the two input currents i_{i1} and i_{i2} are subtracted, and if all current mirrors have unity gain, the resulting gain is $\alpha_I = -2$. A different gain can easily be achieved by changing the width of all output transistors $M[5\text{–}6][1,3]$.

Composite transistors   The transistors with boxes as gates are actually composite transistors. Any "super transistor" configuration can be used, but simple cascodes as shown in Fig. 6.4 provide sufficient voltage swing, since the voltage swing over the MOSFET resistors critically determines the harmonic distortion of the filter. The higher output resistance of regulated cascode transistors is not needed either, since the output is already capacitive in the frequency region of interest. As discussed in Sec. 5.5.1, the cascode transistors can be biased with the mid-rail voltage V_m. The voltage difference ΔV was explained in Sec. 5.5.1, it sets the possible voltage swing at the Z output; $\Delta V = 0$ is the optimum choice for the charge-pumped filter described in Sec. 5.5.1 and Sec. 7.4.2.

Bias circuit   It is apparent that the cascode transistor of $M\,11$ cannot be biased by V_m, since the gate voltage of $M\,12$ is too low. Fig. 6.3 shows the bias circuitry which generates the bias voltages for both half-circuits. The voltage generated by the single transistor $M\,81$ biases the cascode transistors of $M\,11$ and

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[1]The notation $M[1\text{–}6]3$ denotes "all $M\,i3$, where $i = 1\ldots6$."
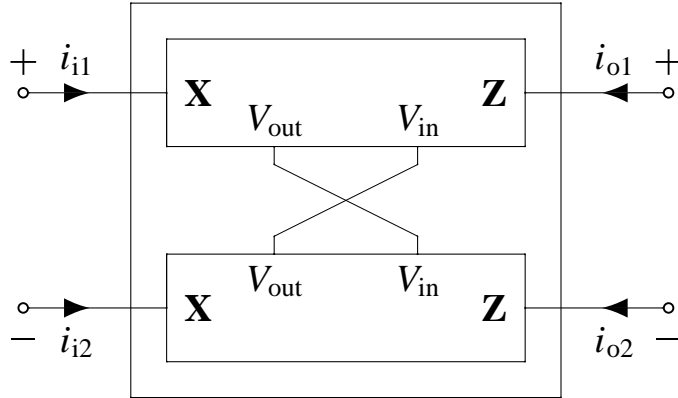
Balanced current amplifier (CCII). **Figure 6.1**
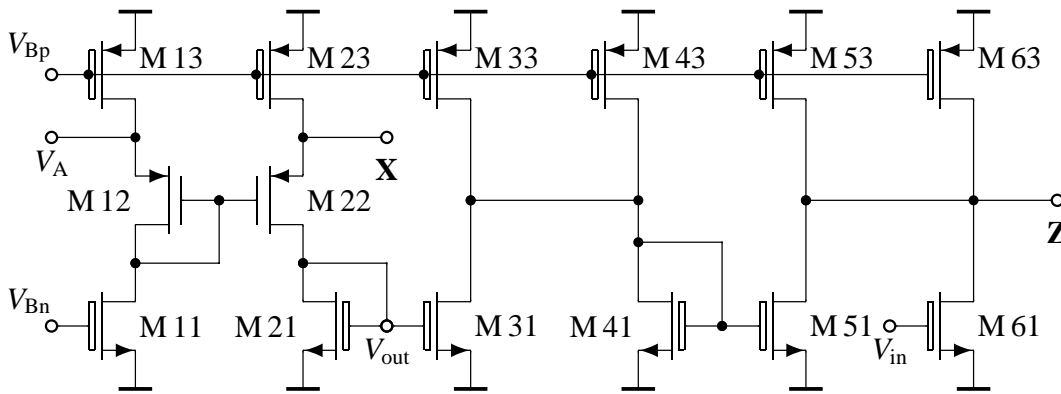
Half circuit of the current amplifier. **Figure 6.2**
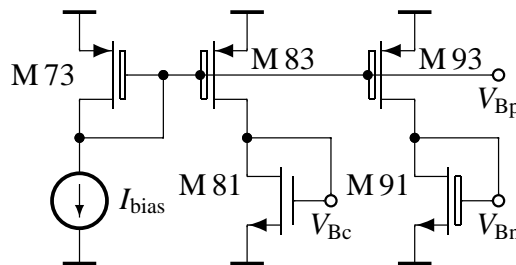
Bias circuit. **Figure 6.3**
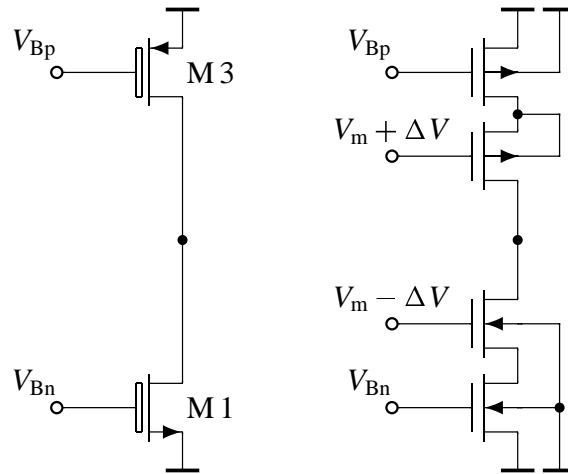
Figure 6.4   *Composite transistors used in the current amplifier.*

M 91. For all test circuits, the current source I_{bias} is located off-chip (c.f. Chap. 7).

6.3.2   Noise analysis

White noise

The white noise of the current amplifier can be calculated by referring the noise current contributions of all transistors to the Z output of the current amplifier. Since there are defined relationships between most of the transistors in the current amplifier, it is possible to express all noise contributions in terms of the white noise spectral density of M 33's drain current,

$$(6.2) \qquad\qquad i^2_{\text{M}33} = 4\hat{k}T \cdot \frac{2}{3}\alpha_{\text{p}}\,g_{\text{m}33}\,,$$

where α_{p} is a noise correction factor (see Tab. 5.1) [Tsividis96]. The noise contributions of all transistors at the Z output of the current amplifier can then be added, but note that the noise of a single transistor travelling along paths with different signs will *not* cancel at the output because the different paths have different time delays.

Keeping the width of the bias transistor and the ratio of the aspect ratios of M 22 and the aspect ratio of M 33 as free parameters, we obtain

(6.3)

$$i_{\mathrm{CCCS}}^2 = 2i_{\mathrm{M}33}^2 \left(\alpha_{\mathrm{I}}^2 \left[\frac{\alpha_{\mathrm{n}}}{\alpha_{\mathrm{p}}} \sqrt{\frac{L_{22}}{W_{22}} \frac{W_{33}}{L_{33}}} + \frac{3}{2} \left(1 + \frac{\alpha_{\mathrm{n}}}{\alpha_{\mathrm{p}}} + \sqrt{\frac{W_{73}}{W_{33}}} \right) \right] \right.$$
$$\left. + \frac{\alpha_{\mathrm{I}}}{2} \left(1 + \frac{\alpha_{\mathrm{n}}}{\alpha_{\mathrm{p}}} \right) + 2\sqrt{\frac{W_{73}}{W_{33}}} \right).$$

In the current amplifier used in Sec. 7.3.2, this is approximately $160\,i_{\mathrm{M}33}^2$. Of this noise, 70 % are produced by current mirrors and current sources, 20 % by the input transistors M 12 and M 22, and 10 % by the bias transistor M 73. This results in $i_{\mathrm{CCCS}} = 36\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$.

The white noise of the current amplifier is then shaped by the filter in which it is used, the filtered noise can be calculated approximately using the noise bandwidth of the filter, f_{x} [Johns97, Chap. 4]:

<div style="text-align:right">Shaped noise</div>

(6.4) $$i_{\mathrm{Filter\,(RMS)}}^2 \approx i_{\mathrm{CCCS}}^2 \cdot f_{\mathrm{x}} \,,$$

where f_{x} can be derived from the filter's ideal transfer function:

(6.5) $$f_{\mathrm{x}} = \int_0^\infty \left| \frac{1}{-\frac{f^2}{f_{\mathrm{p}}^2} + j\frac{f}{f_{\mathrm{p}} q_{\mathrm{p}}} + 1} \right| \mathrm{d}f = \frac{\pi}{2} q_{\mathrm{p}} f_{\mathrm{p}} \,.$$

Note that the same f_{x} results for the second-order bandpass filter.

This result corresponds well to measurements, as Fig. 6.5 shows. The measurements in this figure were made with the biquad described in Fig. 7.3.3. Note how close the calculated $i_{\mathrm{CCCS}} = 36\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$ is to the measured $45\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$. The curve denoted by "$i_{\mathrm{shaped}}$" is the CCCS's noise shaped by the filter transfer function, while "i_{Filter}" is the measured filter noise spectral density. The two curves agree closely, which means that the noise contribution by the passive network is negligible.

<div style="text-align:right">Measurement results</div>
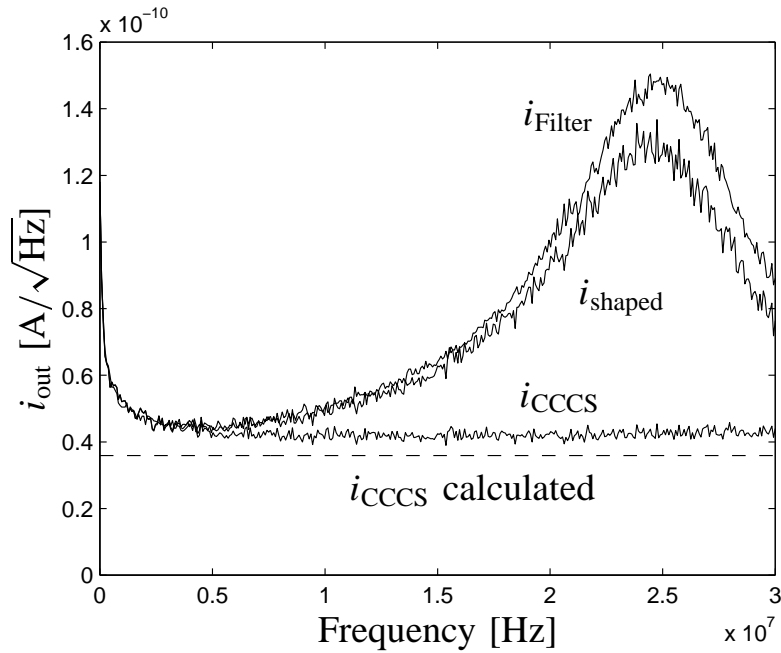
Figure 6.5   *Output-referred noise-power spectral densities.*

6.3.3   Trade-offs

Signal swing vs.
SNR

The choice of V_m and ΔV determines the spurious-free dynamic range of the filter in which the current amplifier is used. Increasing ΔV reduces the harmonic distortion of the filter, but increases the noise, as discussed in Sec. 5.5.1.

R_{in} vs. SNR

The X-input resistance is $R_{in} \approx 1/g_{m22}$ and can thus be decreased by making M 22 wider and by increasing the bias current. If the bias current is increased, then the sizes of all current-mirror transistors must be increased as well in order to maintain voltage margins and voltage swings. This increases the Z-output capacitance of the current amplifier and also the noise. On the other hand, increasing the bias current also moves the parasitic poles and zeros to higher frequencies and thus reduces the phase lag of the current amplifier.

Limit on maximum
output capacitance

If the current amplifier is used to build an SAB with a certain f_p, q_p, and stop-band attenuation A_{stop}, then it is advisable to choose the bias current as small as possible and make M 22 as wide as possible, such that the resulting R_{in} and the resulting phase lag are still acceptable (c.f. Sec. 4.4). In the extreme case, the current-mirrors can be designed such that the Z-
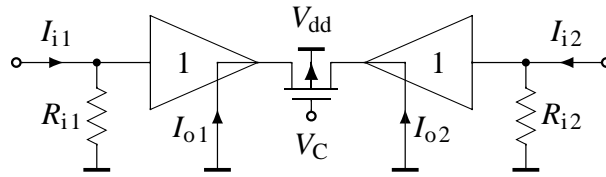
Concept of a variable-gain current amplifier.　　　**Figure 6.6**

output capacitance acts as a signal capacitance, as was shown in Sec. 5.6.4.

Variable-gain current amplifier　　　6.4

The way of thinking used throughout this thesis to build tunable SABs is to use amplifiers consisting of simple, interlinked buffers together with MOSFET resistors to obtain adjustable or tunable circuits. The same technique can also be applied to building a tunable current amplifier. In this section, we first discuss the test circuit from [Schmid99b], which was the core of a variable-gain current amplifier, and then we present a full-grown tunable current amplifier that was developed using the knowledge we gained from the test circuit.

Design idea

Core of a variable-gain current amplifier　　　6.4.1

The concept of our variable-gain is shown in Fig. 6.6. Like the current amplifier discussed above, it is completely symmetrical. The input current $I_{i1,2}$ flows through a poly-silicon resistor $R_{i1,2}$, and the resulting voltage is buffered. The voltage difference over the MOSFET resistor causes a current to flow out of one voltage buffer and into the other. Both currents $I_{o1,2}$ are sensed and mirrored to high-impedance outputs. The overall current gain can then be adjusted almost linearly by varying the control voltage of the MOSFET resistor.

Concept

The idea of implementing a transconductance amplifier by connecting two voltage buffers to a simulated resistor was presented in [Kwan91], but there a six-transistor resistor was used. However, using a single MOSFET resistor is sufficient,

Effects of using a MOSFET resistor
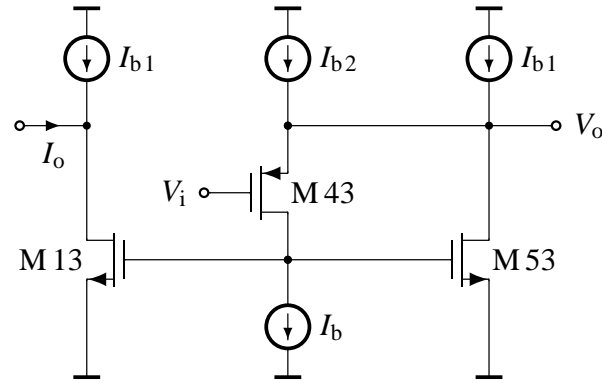
Figure 6.7   *Voltage buffer with level shift.*

provided that the voltage over it is purely differential mode. If such a pure differential-mode voltage signal is applied to a strongly inverted MOSFET operating in the linear region, it will theoretically cause a distortion-free channel current [Tsividis86]. Any remaining common-mode signal will be rejected almost completely, since it is the voltage *difference* which is converted into a current. However, simply stating that the common-mode rejection ratio is very high would be misleading, since a common-mode signal changes the resistance of the MOSFET resistor and therefore *modulates the amplitude of the differential-mode signal.*

Voltage level shifter   It is advantageous to make the voltage difference between the MOSFET's gate and channel as large as possible. In contrast to the MOSFET–C filters, the MOSFET resistors are not connected to any external nodes in the tunable current amplifier. Thus the signal ground can be chosen freely. This makes it possible to use *p*MOS resistors again in conjunction with voltage buffers that shift the signal ground as far away from the lower rail (i.e. the gate control voltage of the resistor) as possible. We chose the same buffer that was used in [Kwan91]; it is shown in Fig. 6.7. Transistor M 43 is biased with a constant current I_{b2}. This makes its gate-source voltage approximately constant as well, and it acts as voltage buffer with a voltage level shift of approximately 1.25 V in our implementation. Any current flowing through the terminal 'V_o' is conducted by M 53, which is biased with I_{b1}. This current is then mirrored by M 13 and provided at the high-impedance output 'I_o'.
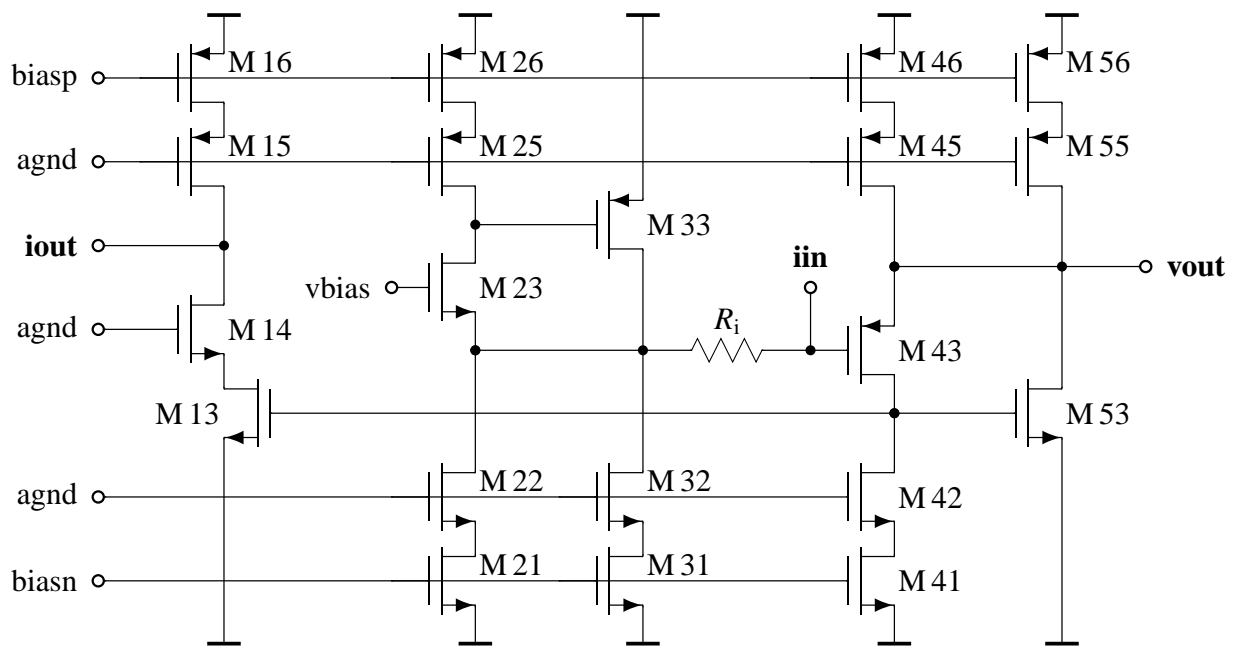
Half-circuit of the variable-gain current amplifier.   **Figure 6.8**

The same voltage buffer is used a second time in the circuit, namely to provide the signal ground to which R_i is connected. Connecting it directly to the analogue-ground ('agnd') line on the chip would be a bad idea, since the signal current injected into that line would cause a voltage drop at the bonding wires. As a result, the 'agnd' line would bounce and feed interfering signals into every other component on the chip using analogue ground as a reference voltage. The variable-gain current amplifier therefore consists of four voltage buffers, several constant current sources providing the currents $I_{b1,2}$, two current mirror output stages, and a single MOSFET resistor.

Grounding the poly resistor

The schematic of the half-circuit is shown in Fig. 6.8. The bias voltage applied to 'vbias' is buffered, with a negative level shift, by the first voltage buffer M[2,3][1–6]. M23 provides the voltage buffering function, M33 collects the current applied to 'iin', and the other transistors form constant current sources supplying the bias currents $I_{b1,2}$. The voltage drop over the poly-silicon resistor R_i is then copied to 'vout', the terminal connected to the MOSFET resistor, by the voltage buffer M[4,5][1–6] from Fig. 6.7. M1[3–6] form a class A current mirror together with M53. Since the drain voltage of M13 is always lower than the drain voltage of M53, the former should be made a bit wider than the latter to compensate for

Description of the circuit
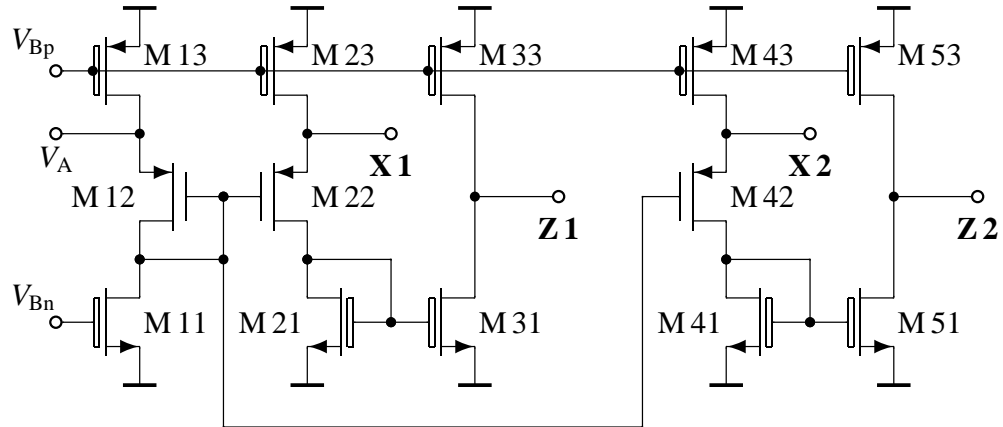
Figure 6.9   *Input buffer of the variable-gain amplifier.*

systematic offset. All cascode transistors can be biased by analogue ground if the amplifier is to be used in a charge-pump-controlled filter (see Sec. 5.5). The voltage applied to 'vbias' is approximately 1.1 V above analogue ground and sets both the signal ground at the current input and the operating point voltage at the MOSFET resistor's terminals, which is about 1.2 V above 'agnd' in our implementation (see Sec. 7.3.4 for more information).

6.4.2   Complete variable-gain amplifier

Input buffers

In order to be used in MOSFET–C filters, the input currents of the amplifier core must be buffered. This can be done using the structure shown in Fig. 6.9. It is actually the fixed-gain current amplifier described in Sec. 6.3 without the differencing circuits, with the two signal paths sharing a common input level shifter, and with the same biasing circuit. More information on transistor sizing and performance will be given in Sec. 7.4.4.

The use of this concept in the literature

Finally, it should be remarked that another group of authors recently published a transconductor that is very similar to our amplifier core, without the input resistors, and with a real resistor instead of a MOSFET resistor. The authors also show additional linearisation circuitry and use the very linear transconductor to build a Gm–C filter that is tuned with capacitor matrices [Lindfors99].

Conclusion   **6.5**

The current amplifiers introduced in this section are built as   Common-mode
simple as possible, and they do not have special common-mode   rejection
rejection circuitry, which makes them fast and power-efficient.
The measurement results obtained with the 7th-order filter (c.f.
Sec. 7.4.3) show that the inherent common-mode rejection of
every biquad stage (the amplification of a difference of input
currents) is sufficient to drive the next biquad in the cascade.
Nevertheless, the question remains open how much could
be gained by improving the common-mode rejection of the
amplifiers.

The fixed-gain current amplifier is derived from a well-known   Open questions
structure, and there is little room for improvement, but the
variable-gain amplifier is not much more than a first attempt
to build such an amplifier using a MOSFET resistor. Two
possibilities for future research are to increase the linearity of
this amplifier by adding common-mode rejection circuitry and
by using better voltage buffers.

Chapter 7

Description of test chips and measurements

**In electrical engineering,
Zero and Infinity do not exist,
and Pi equals three.**

(Jean Weiler)

This chapter provides those measurements of the test circuits on our two chips that were not already used in one of the previous chapters. It also describes all circuits (including the off-chip measurement electronics), the component values and dimensions, and discusses some of the design decisions we made. Chip photos give an impression of the symmetrical and compact layout of the test circuits. In addition, some mistakes that were made on the chips are also mentioned.

7.1   Background

I came to the Signal and Information Processing Laboratory with the plan to become an Analogue-IC designer. Little did I know back then that the main problems of analogue-IC design would not be theory, design, and layout, but mastering the design kits, understanding what the circuit simulators do, and measuring the chips. I brought no experience in analogue design with me; this thesis was only possible because of the marvellous support I got at this laboratory. There were two experienced IC designers here, Markus Helfenstein and Drahoslav Lím, who taught me the use of the design kits and the simulators. In addition, our EE department also has a Microelectronics Design Centre, whose members Andreas Wieland and Christoph Balmer solved many problems I had with Cadence and AMS's design kits. Last, but not least, Felix Frey, the specialist for high-frequency electronics working at our laboratory, built for me the printed-circuit board I needed for the measurements and taught me how to use the measurement equipment properly, and Thomas Schaerer, our electronics engineer (Elektroniker) helped me with electronics problems after Felix Frey had left the laboratory. Without them, this thesis would have been a theoretical one.

In spite of all this help, I made several mistakes. On the first chip, the coupling between the input pins and the output pins of the chip was so bad that the measurements without calibration were of little use. So although the chip was good enough to give insight and academically interesting measurements, it would not have worked in an actual product. The same happened with another chip that was fabricated at the same time by another doctoral student at our laboratory.

Between the production runs of the first and the second chip, AMS changed the properties of their 0.6-micron CMOS process, including the design rules. What they did not change was the design kit library containing the analogue pads. Every single pad caused several hundred design rule violations, and it was not possible to simulate the chip with these pads. This was, by the way, already

the case for the first chip, back then AMS told me that the pads would work fine on silicon, and they told me the same for my second chip. They were right, but I made a stupid mistake. The pads I used had protection diodes to both rails; I assumed, without checking, that the diodes only went to the substrate, because I simply did not know then that it could be otherwise. The effects this had on the chip and how I could solve this problem are both described below.

All this was very exciting and interesting, but of course I wonder what will go wrong on my next chip.

Measurement electronics 7.2

This section describes the circuits that were used to measure the second test chip. Similar circuits were used to measure the first chip, they are omitted for the sake of brevity. Both circuits were selected, designed and built by Felix Frey according to our specifications.

Outline

Input voltage generator 7.2.1

For all measurements, the chips were driven by the single-ended to balanced voltage converter shown in Fig. 7.1. It has a 50-Ω input to which the generator of the network analyser can be connected and provides precisely balanced output voltages. It bases on the CFB opamp AD 8002, which is well capable of driving the pads of our chip. Actually, the circuit in Fig. 7.1 is an adaption of a differential line driver proposed in the data sheet of the AD 8002. The conversion gain is one, and since the network analyser expects a resistance of 50 Ω, there is only the 6-dB loss of the power splitter at the analyser output to be taken into account when setting the power of the analyser.

Balanced line driver

On the first chip, every test circuit still had its own off-chip input-voltage converter; on the second chip, only one converter was used to drive all circuits at once. This was possible since every circuit could be switched off completely by setting its bias current to zero, and it had the additional advantage that

Difference between chip 1 and chip 2
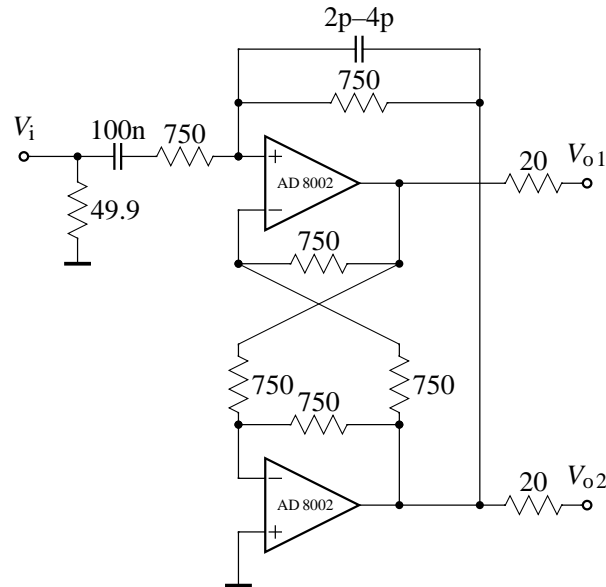
Figure 7.1   *Single-ended to balanced voltage converter*
using AD 8002 CFB opamps.

enough chip pads were still free so that the inputs could be
decoupled from each other and from the rest of the pads by
placing grounded pads in between.

7.2.2   Output I–V converter

Two-stage
transresistance
amplifier

The current output of every test circuit was converted to a
single voltage by the circuit shown in Fig. 7.2. It consists of
tow independent I–V converters based on the AD 8011 (another
CFB opamp) that has an $R_m = 750\,\Omega$. The following stage is
a difference amplifier based on the AD 8002 with a voltage
gain of 5. Together with the differencing, the overall R_m from
a single current output to the converter output is $7500\,\Omega$. The
reason that two different CFB opamps were used is that the
AD 8011 is basically slower; because of the stability problems
that often occur with high-speed amplifiers, it is not advisable
to use amplifiers that are faster than necessary.

7.2.3   Measurement equipment

Brief description

All transfer functions and characteristics were measured with
the 500-MHz spectrum analyser HP 8751 A; the noise and
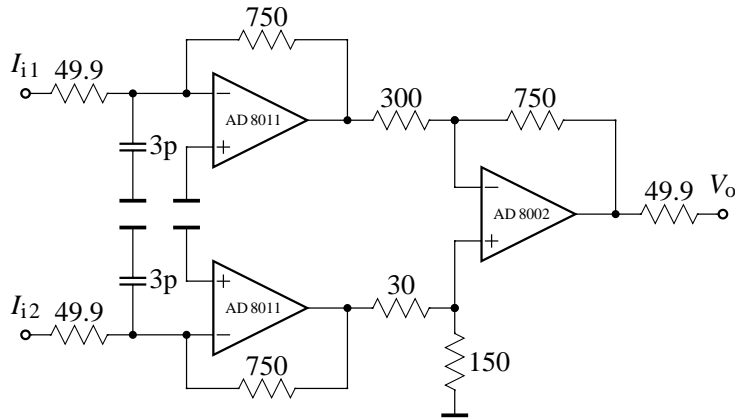
*Balanced-current to single-ended voltage converter
using AD 8002 and AD 8011 CFB opamps.*

Figure 7.2

clock feed-through was measured with the 150-MHz spectrum
analyser HP 3588 A. For the harmonic-distortion measure-
ments, a 2-V_{pp} was generated with the Tektronix AFG 2020
function generator and then attenuated by a programmable
attenuator, the Marconi MA 2186, in order to produce a
harmonically clean signal for the measurements.

First test chip 7.3

V–I converter and signal inputs 7.3.1

Every circuit on the test chip that has a balanced current input
is driven by an on-chip V–I converter that converts the balanced
voltage input into a balanced current. The reason that such
a converter is necessary is that otherwise the pad capacitance
and the input resistance of the circuit would form a pole at
unacceptably low frequencies (several MHz). This looks like a
disadvantage of current-mode filters, but a voltage-mode filter
that has an output impedance equal to the input impedance of
the current-mode filter would simply have the same problems
at its output, where a voltage buffer would have to be inserted.

*Why an on-chip V–I
converter is needed*

On this first chip, two major mistakes were made. First, every
circuit on the chip had its own pair of input pads. There
were not enough pads remaining to isolate the input pads
electromagnetically. As a result, there was a considerably

*Major mistakes on
the first chip*

#	main transistors	cascode transistors
M [1–4]1	45×3 µm	80×0.6 µm
M [5–6]1	57.3×3 µm	104×0.6 µm
M 81	37.3×3 µm	—
M 91	45×3 µm	80×0.6 µm
M [1–2]2	120×0.6 µm $\times$ 2	—
M [1–4]3	120×3 µm	200×0.6 µm
M [5–6]3	200×3 µm	260×0.6 µm
M [7–9]3	120×3 µm	200×0.6 µm

Table 7.1   *Transistor dimensions. '$\times$ 2' denotes devices in common-centroid layout.*

strong electromagnetic signal path from the inputs to the outputs of the chip. Second, the V–I converter used on the chip was too complicated, required an input voltage offset and also was comparatively slow. Since we do not consider the idea behind it useful, we omit it here for the sake of brevity and recommend the V–I converter described in Sec. 7.4.1.

Calibration measurements

The two mistakes together made it only possible to obtain measurement results by calibrating the non-idealities out, which was possible because the V–I converter alone was available on the chip for use as a reference path. The differences between the calibrated and the uncalibrated signals were very large, but not so large that measurements became impossible: the coupling acted as a 20-MHz high-pass filter in parallel to our filter and thus affected only the transfer function measuerements.

7.3.2   Current amplifier

It could have been built smaller

The current amplifier was built as described in Sec. 6.3 using the transistor and capacitor dimensions shown in Table 7.1. It turned out that the balancing of the two signal paths through the current amplifier was more than precise enough. Thus the width of all 3-µm transistors could be reduced to 1.8 µm on the second chip. The design decisions that are necessary to obtain the transistor sizes will be explained in Sec. 7.4.2, where a structurally identical current amplifier with better chosen transistor sizes is discussed.

#	capacitor dimensions	capacitance
C [1–2]2	$13.6 \times 13.6 \ \mu m \times 10$	1.0 pF
C [1–2]4	$13.6 \times 13.6 \ \mu m$	0.1 pF

#	MOSFET resistors
R [1–2]1	$22 \times 2.4 \ \mu m \times 2$
R [1–2]2	$22 \times 1.9 \ \mu m \times 2$

Capacitor and resistor dimensions. **Table 7.2**

Pair of biquadratic filters 7.3.3

Description of the layout

The current amplifier described in the previous section was used to build a second-order filter as described by Fig. 5.4 with the dimensions of the passive elements given in Tab. 7.2. A chip photo is shown in fig. 7.3, the current amplifier (CCCS), the passive elements, and the empty space left of the capacitor array have a total size of $320 \times 340 \ \mu m$, or $0.11 \ mm^2$. On the photo, the careful layout of the capacitors containing unit capacitors and dummy elements can be seen. As it turned out, mismatch-induced effects were comparatively small, so the complex layout of the capacitors was not really necessary and was not used anymore on the second chip (c.f. Sec. 7.4.2).

Measurement results

Measurements were made for this filter; some of them were shown in previous sections, and most were published in [Schmid99b] and [Schmid00d]. The filter consumes 12.4 mW from a 3.3-V power supply. The pole frequency of the filter is tunable from 18 MHz to 24 MHz, with a pole Q a bit higher than 3. Due to the inappropriate choice of the analogue ground, as described in Sec. 5.4.1, the SNR at 1 % of harmonic distortion was only 29 dB, would have been 33 dB at the top of the tuning range if the analogue ground had been chosen properly, and could have been extended to 35...37 dB by changing the bias voltages of the cascode transistors at the current amplifier and moving the analogue ground further towards the positive rail.

Inter-chip matching

The inter-chip standard deviation of the pole frequencies was 1.5 % for 14 measured chips from the same process run, and 3 % for the pole quality factor. The latter is more than precise enough for most video-frequency applications. It would have
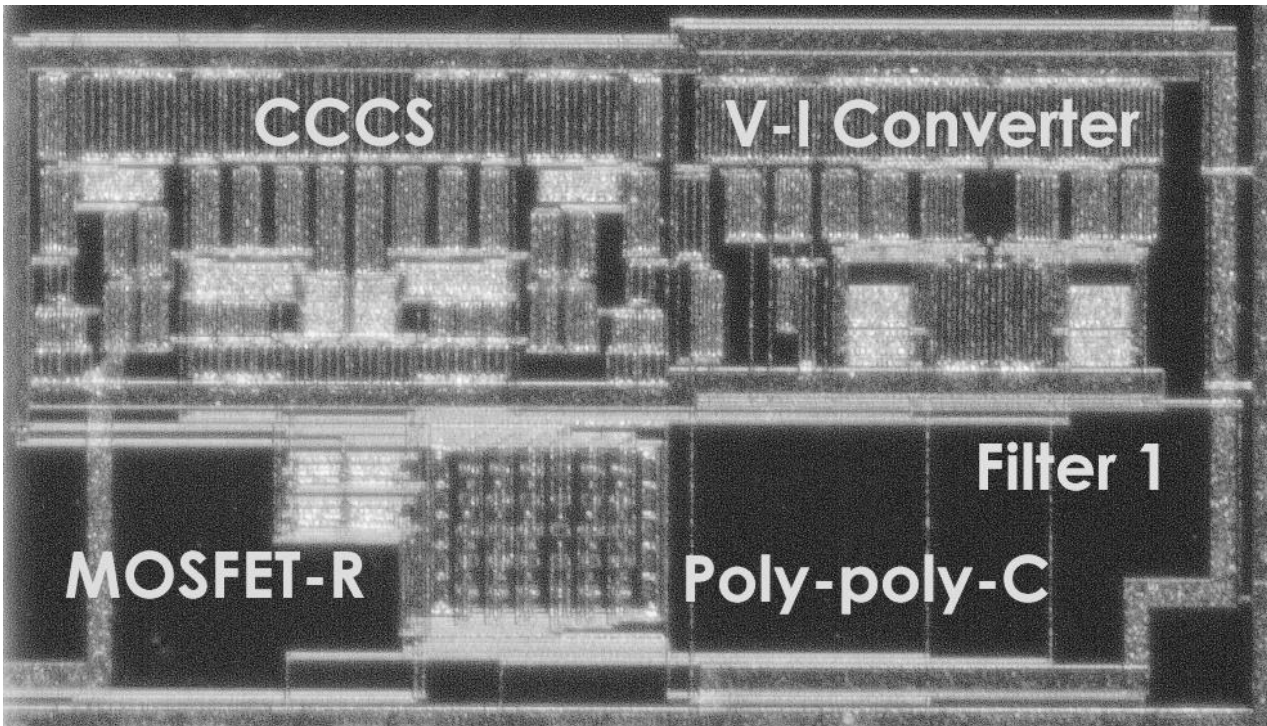
Figure 7.3   *Photo of the biquadratic filter.*

been interesting to obtain on-chip matching results. In order to achieve this, two "identical" biquads were placed on the same chip. Although the standard deviations were the same in both cases, the pole frequency of one of the filters was 7 % lower, and its pole quality factor was 2.5 instead of 3. We never found out why this was so. Since the effect was absent in all simulations, we think that the pads have something to do with it. As mentioned above, we could not simulate the chip with the pads due to bugs in the design kit.

Discussion

These measurements show that MOSFET–C SABs like the one on chip 1 are probably useful only for applications that require a comparatively low SFDR, like signal-shaping filters in hard-disk read channels. If a higher SFDR is required, a charge-pumped filter like the one described in Sec. 7.4.2 should be used.

7.3.4   Variable-gain current-amplifier core

Description and
measurements

The core of the variable-gain current amplifier was implemented with the element sizes shown in Tab. 7.3. A chip

Transistor	Dimensions
M [2–4]1	$100 \times 1.8 \ \mu m$
M [2–4]2	$96 \times 0.6 \ \mu m$
M 13	$130.8 \times 1.8 \ \mu m$
M [2,5]3	$126 \times 1.8 \ \mu m$
M [3,4]3	$200.1 \times 1.2 \ \mu m$
M 41	$120 \times 0.6 \ \mu m$
M [1,2,4,5]5	$224 \times 0.6 \ \mu m$
M [1,2,4,5]6	$300 \times 1.8 \ \mu m$
MOSFET-R	$12 \times 3 \ \mu m$
$R_i = 12.46 \ k\Omega$	

Element sizes used in the variable-gain current-amplifier core.   **Table 7.3**
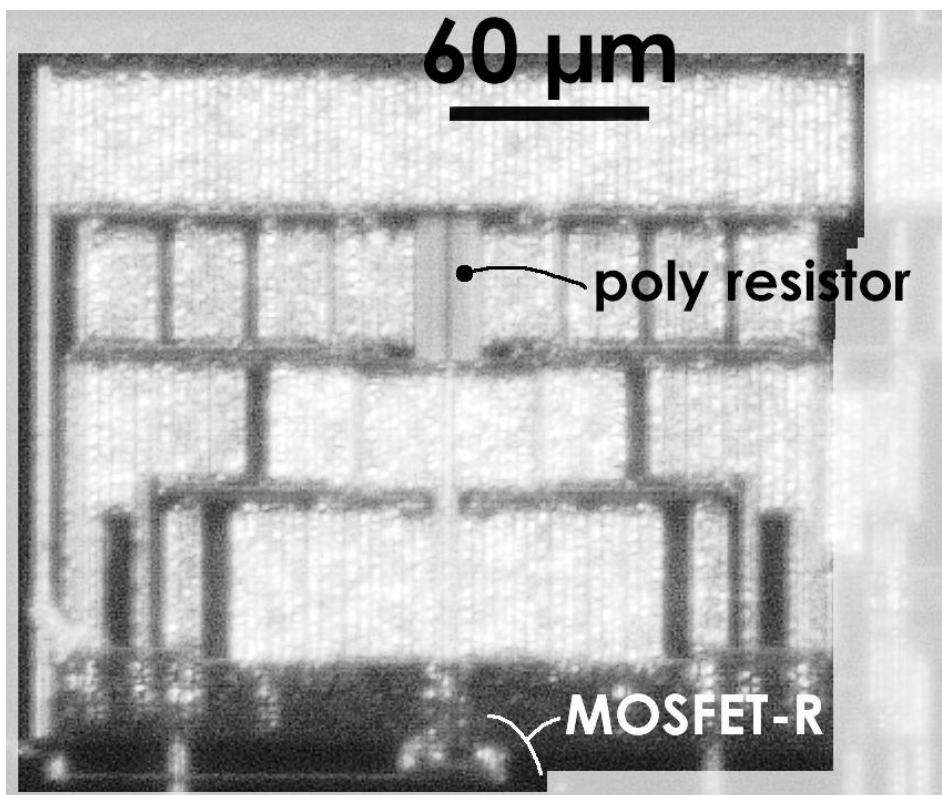
Photo of the amplifier core.   **Figure 7.4**
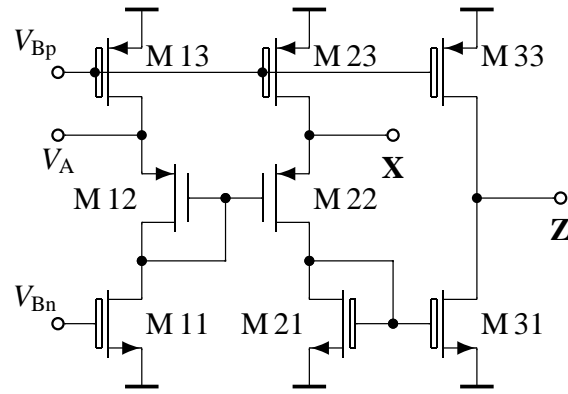
Figure 7.5   *Current amplifier used in the V–I converter.*

photo is shown in Fig. 7.4, where the poly-silicon resistors and the MOSFET resistor can be seen. The test circuit covers an area of $0.07\,\text{mm}^2$, and the bias currents are $I_{b1,2} = 375\,\mu\text{A}$. Measurement results of this circuit were given in [Schmid99a]. There it was shown that a full current amplifier would be able to drive a MOSFET–C filter with a pole frequency of 900 kHz and an SFDR of $-45\,\text{dB}$, with a power consumption of 12.4 mW. An improved version of this amplifier performs better, as will be shown in Sec. 7.4.4.

7.4   Second test chip

7.4.1   V–I converter and signal inputs

Description

The V–I converter used on this chip simply consisted of poly-silicon resistors connected between the pad and the input of the current amplifier shown in Fig. 7.5. The conversion resistances (i.e. the $1/g_\text{m}$) of these converters were $20.3\,\text{k}\Omega$ for the 7th-order filter and $6.78\,\text{k}\Omega$ for all other test circuits. The converter has the same transistor sizes that are given in Tab. 7.4, and a bias current of $160\,\mu\text{A}$.

Noise and distortion

The transconductance of the V–I converter is shown in Fig. 7.6. Its g_m is almost constant up to 50 MHz, but its phase lag reaches comparatively high values in the region of the pole frequencies of our filters. Both effects can, however, be cancelled out for all other measurements by calibrating the network analyser to
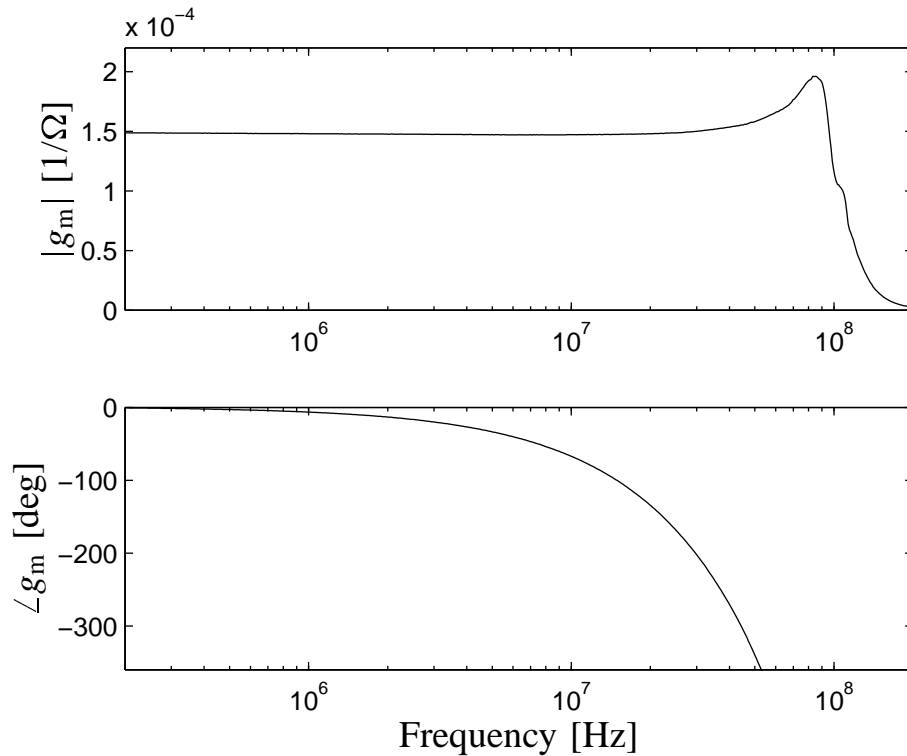
Measured transconductance of the V–I converter.   **Figure 7.6**

the V–I converter that is supplied on the chip as a reference path. Measurements showed that the harmonic distortion introduced by the V–I converter is negligible, but its noise is not. For example, it adds about 4 dB of noise to the biquads, but only about 1 dB to the 7th-order filter. This contribution was subtracted from the measurements presented below.

Charge-pumped biquad   7.4.2

The structure of the current amplifiers used in this biquad is the same as on chip 1 (see Sec. 6.3). All transistor and capacitor dimensions are shown in Tab. 7.4 (c.f. Fig. 5.4). We will now briefly point out some of the reasons why the transistor dimensions were chosen as shown in Tab. 7.4. In the composite transistors, the W/L ratio of the main transistor is about six times smaller than the W/L ratio of the cascode transistor. As was shown in [Burger96], simple cascodes are fastest when the V_{dsat} of the cascode transistor is about 40 % of the V_{dsat} of the main transistor. The factor of six results if the W/L ratios are calculated from V_{dsat} and I_d.

Design decisions

	capacitor dimensions	capacitance
C [1–2]2	46.3 × 28 μm	1.13 pF
C [1–2]4	7.4 × 28 μm	0.19 pF

	main transistors	cascode transistors
M [1–6]1	45 × 1.8 μm	95 × 0.6 μm
M 81	14 × 0.6 μm	—
M 91	45 × 1.8 μm	95 × 0.6 μm
M [1–2]2	120 × 0.6 μm × 2	—
M 13	87 × 1.8 μm	140 × 0.6 μm
M [2–8]3	70 × 1.8 μm	140 × 0.6 μm
M 93	87 × 1.8 μm	140 × 0.6 μm
R [1–2][1,3]	12 × 6 μm	—

Table 7.4   *Transistor and capacitor dimensions in the charge-pumped biquad.*

The absolute transistor dimensions were found iteratively. First, it was clear from experience that the bias current would have to be around 160 μA to achieve a pole frequency around 32 MHz. The maximum signal current to be supported by the current amplifier was designed to be 60 μA, approximately the current at which the MOSFET resistors would saturate. This determined the sizes of all current source and current mirror transistors. The input transistors M [1–2]2 were designed such that they would provide an X input resistance around 500 Ω, and then it was verified that the cascode transistor in M 11 would indeed remain in saturation by giving it a bias voltage 0.1 V below analogue ground, which determined the size of M 81. Finally, the sizes of the passive elements were calculated from first-order formula and corrected through iterative simulations and corrections, where the last corrections were made on post-layout simulations. Note that C [1–2]4 is small compared to the output capacitance of the current amplifier. This capacitance could even have been omitted, as was shown in Sec. 5.6.4.

Layout mistake   The gate control voltages of this filter are generated by the charge pump described in Sec. 5.5.2, whose comparatively large charge tank can be seen at the bottom left of Fig. 7.7. The rest of the charge pump elements is below the tank; above
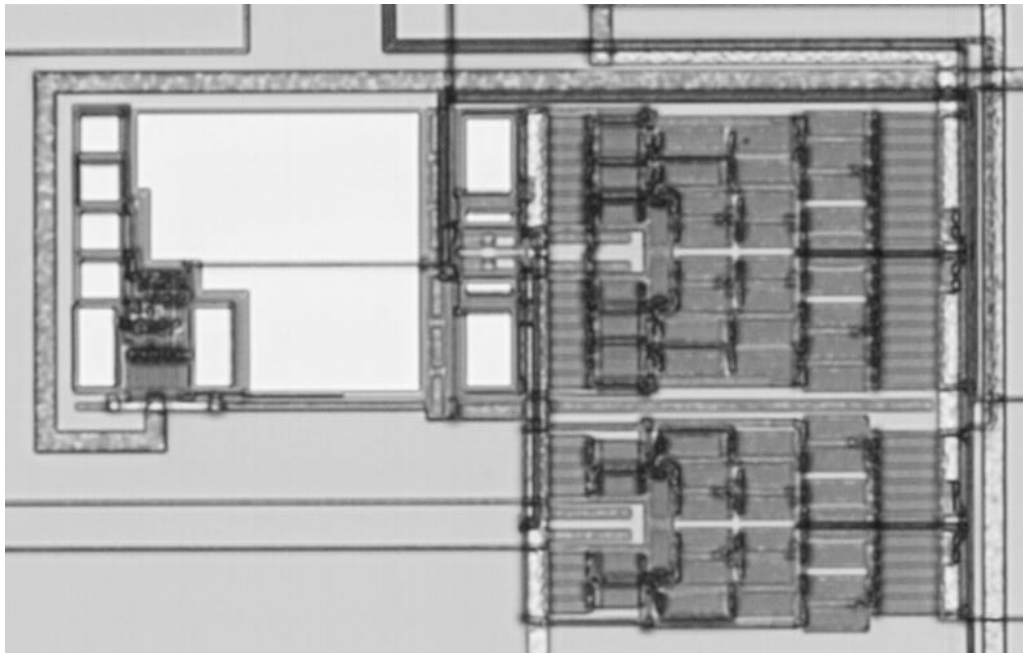
Photo of the charge-pumped biquad. Top left: charge pump.
Top right: biquad. Bottom right: On-Chip V–I converter.

<div style="text-align:right">**Figure 7.7**</div>

the tank, the filter capacitors appear as bright rectangles, with
the small MOSFET resistors in between. The symmetrical
structure above the passive elements is the current amplifier,
to the right of it, the active part of the V–I converter can be
seen. As was pointed out in Sec. 5.5.3, putting the charge
pump so close to the passive filter elements that the filter output
lines had to be drawn on top of the guard bar was a bad idea,
since then the substrate noise could leak through to the output.
With a proper layout, this would not have happened, as was
discussed in Sec. 5.5.3 as well.

Adjusting the charge pump supply voltage from 2.7...3.3 V   Results
tunes the pole frequency from 22.4 MHz up to 36 MHz. The
input current that causes 1 % (-40 dB) of harmonic distortion
varies between 36 μA...165 μA. As discussed in Sec. 6.3.2, the
noise is mainly white noise from the current amplifier shaped
by the filter. The measured SNR of the filter for a signal causing
-40 dB of harmonic distortion varies from 54 dB to 66 dB over
the whole tuning range; an SNR of over 55 dB is reached for
pole frequencies above 23 MHz. The filter consumes 16 mW
from a 3.3-V supply, and covers a chip area of 200×550 μm,
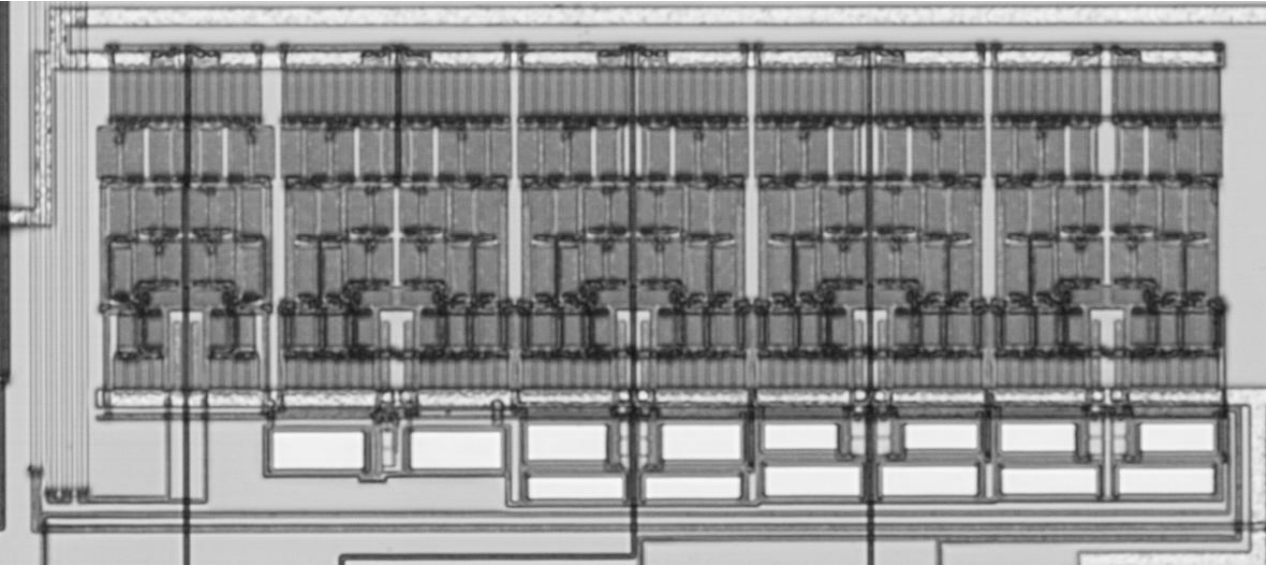
Figure 7.8   *Photo of the 7th-order biquad cascade.*

or $0.11\,\text{mm}^2$, including the charge pump. The biquad alone
covers an area of $200 \times 320\,\mu\text{m}$, or $0.064\,\text{mm}^2$.

7.4.3   8-MHz 7th-order biquad cascade

Description

Using the biquads from Sec. 7.4.2, the 7th-order Bessel
filter shown in Fig. 7.8 was built. From left to right, the
following building blocks can be seen: the poly resistors
(four vertical gray lines) and the current amplifier of the V–I
converter, a passive first-order low-pass filter with a normalised
$f_\text{p} = 1.687$ that consists of a current amplifier and a first-order
MOSFET–C lowpass filter, and three MOSFET–C SABs with
$(f_\text{p}, q_\text{p}) = (2.053, 1.13)$, $(1.719, 0.53)$, and $(1.825, 0.66)$, in this
order. This filter could, e.g., be a pulse equaliser in a $1 \times$ DVD
read channel [Kim98].

Element sizes

When such biquads are cascaded, it must be taken into account
that every biquad presents a resistive load to the previous
biquad. As before, the element sizes that are shown in Tab. 7.5
were first calculated and then refined using simulations. All
current amplifiers were identical to the one used in sec. 7.4.2.
The resulting biquad draws $49\,\text{mW}$ from a 3.3-V supply and
covers a chip area of $700 \times 340\,\mu\text{m}$, or $0.24\,\text{mm}^2$.

(f_p, q_p)		element size	C
$(1.687, -)$	C[1–2]4	$68.9 \times 28\ \mu m$	1.68 pF
	R[1–2]3	$12 \times 8\ \mu m$	
$(2.053, 1.13)$	C[1–2]2	$60 \times 26.75\ \mu m$	1.40 pF
	C[1–2]4	$72.2 \times 16.6\ \mu m$	1.05 pF
	R[1–2][1,3]	$12 \times 6\ \mu m$	
$(1.719, 0.53)$	C[1–2]2	$55.5 \times 19.1\ \mu m$	0.93 pF
	C[1–2]4	$72.2 \times 22.2\ \mu m$	1.40 pF
	R[1–2][1,3]	$12 \times 10.5\ \mu m$	
$(1.825, 0.66)$	C[1–2]2	$56.5 \times 21.25\ \mu m$	1.05 pF
	C[1–2]4	$72.2 \times 19.5\ \mu m$	1.23 pF
	R[1–2][1,3]	$12 \times 9.5\ \mu m$	

MOSFET resistor and capacitor sizes in the 7th-order filter. **Table 7.5**

Tuning range

Fig. 7.9 shows the measured transfer functions of the seventh-order biquad cascade for a tuning voltage $V_C = 4.4\ldots 5\,V$, which corresponds to a charge pump supply voltage of $3\ldots 3.3\,V$. The 3-dB frequency of the filter can be tuned from 4.5 MHz up to 10 MHz.

Distortion

Measurements of the harmonic distortion give curves that look similar to the curves shown in Fig. 5.3. For the tuning range 4.5 MHz...10 MHz, the input current that causes 1 % (-40 dB) of harmonic distortion varies between 14 µA...17 µA.

SNR

Together with the maximum current, the noise spectrum and the noise bandwidth vary as well. As a result, the measured SNR of the filter for a signal causing -40 dB of harmonic distortion remains between 48 dB and 50 dB over the whole tuning range.

Variable-gain current amplifier   7.4.4

Improvement of the core

One of the reasons why the performance of the core was not so satisfying is that the current buffer is not input-output symmetrical. This was changed in the new amplifier, M 33 and M 53 now both have cascode transistors M 34 and M 54, biased with analogue ground like all other cascode transistors. Furthermore, the voltage level shifter in Fig. 6.8 consisting of M [2,3][1–6] was only drawn once, and the poly resistors
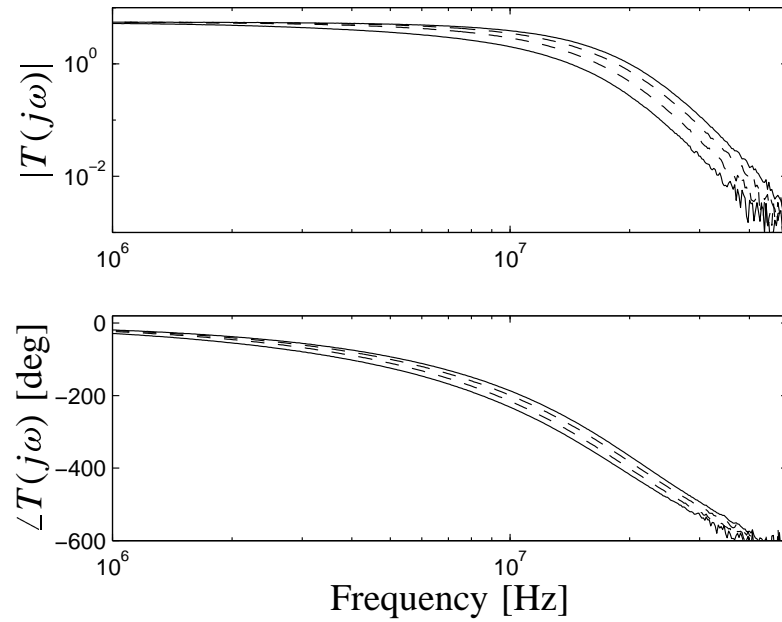
Figure 7.9   *Meaured transfer function of the seventh-order biquad cascade for $V_C = 4.4 \ldots 5\,V$.*

Transistor	Dimensions
M [2–4]1	$45 \times 1.8\ \mu m$
M [2–4]2	$95 \times 0.6\ \mu m$
M [1,5]3	$45 \times 1.8\ \mu m$
M 23	$160 \times 1.2\ \mu m$
M 33	$70 \times 1.8\ \mu m$
M 43	$200.1 \times 1.2\ \mu m$
M [1,5]4	$95 \times 0.6\ \mu m$[‡]
M 34	$140 \times 0.6\ \mu m$[‡]
M [1–5]5	$140 \times 0.6\ \mu m$[†]
M [1–5]6	$70 \times 1.8\ \mu m$[†]
MOSFET-R	$34 \times 2.0\ \mu m$
$R_i = 4.2\,k\Omega$	

Table 7.6   *Element sizes used in the variable-gain current amplifier. ([†]There are three identical, parallel current sources in the branches 2 and 4. [‡]See text.)*

	main transistors	cascode transistors
M [1–5]1	45×1.8 μm	95×0.6 μm
M 81	14×0.6 μm	—
M 91	45×1.8 μm	95×0.6 μm
M [1–4]2	240×0.6 μm	—
M 13	87×1.8 μm	140×0.6 μm
M [2–8]3	70×1.8 μm	140×0.6 μm
M 93	87×1.8 μm	140×0.6 μm

Transistor dimensions in the current buffer (and in the on-chip V–I converter, c.f. Sec. 7.4.1.   **Table 7.7**
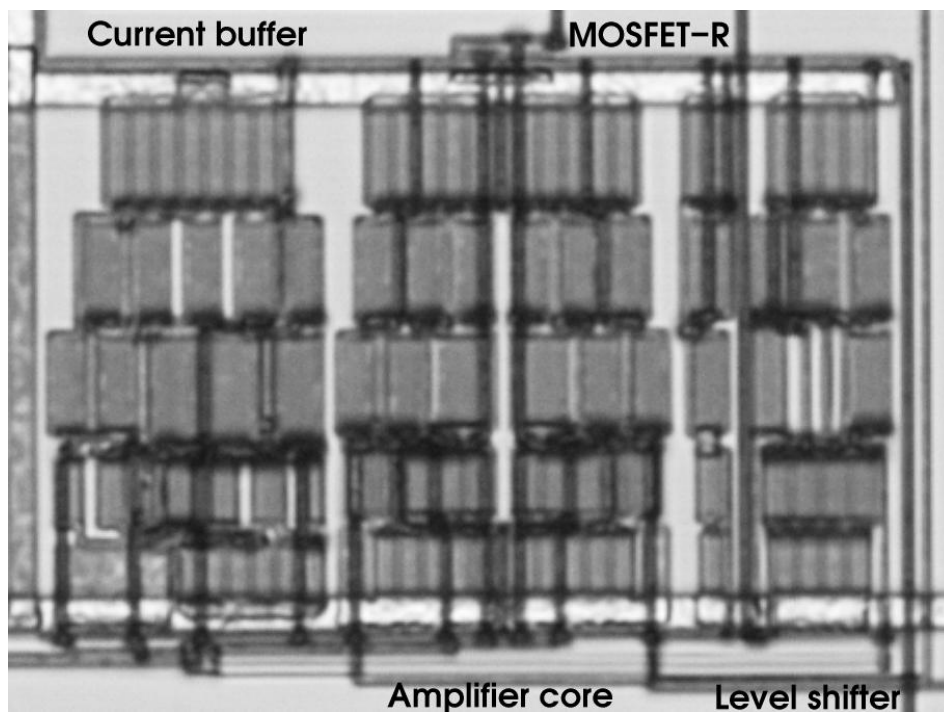
Photo of the variable-gain amplifier.   **Figure 7.10**
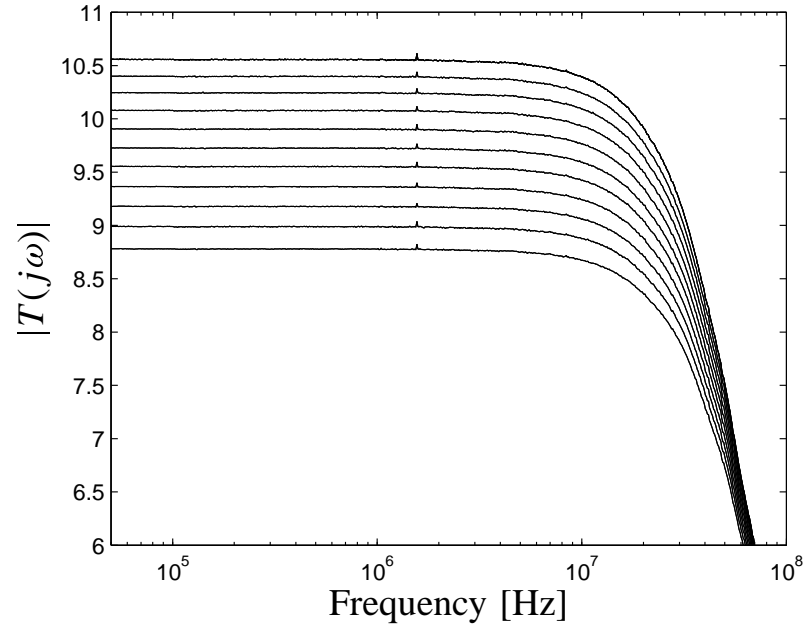
Figure 7.11   *Measured transfer function of the variable-gain current.*

of both half-circuits of the core were connected to its output. The resistance level was also lowered in order to increase the maximum possible input current by setting $I_{b2} = 3\,I_{b1}$, which was done by using three identical copies of the current sources in the branches 2 and 4. The element sizes of the core (Fig. 6.8) and of the input buffer (Figs. 6.9 and 6.3) are shown in Tabs. 7.6 and 7.7, respectively. The design considerations made for obtaining the transistor sizes are very similar to the ones described in Sec. 7.4.2.

Measurement results   This amplifier is driven with a bias current of 160 μA, which means that it draws 12.2 mW from a 3.3-V supply, almost the same as the fixed-gain current conveyor. It covers a chip area of 340×250 μm, or 0.085 mm². The transfer functions for $V_C = 0 \ldots 1.0$V are shown in Fig. 7.11. The DC gain varies in the range $10.6 \ldots 8.8$. (Actually, the gain should have been tunable around 2.0, which it was according to the models we had when we designed the chip (c.f. Sec. 5.3). The 3-dB bandwidth is almost not affected by the tuning and remains at 50 MHz. The phase lag reaches $-20°$ at about 10 MHz, which means that this amplifier can be used to build MOSFET–C filters with adjustable q_p and an $f_p \leq 10$ MHz. The current at which the measured THD reaches -40 dB actually *increases* from 27 μA to 30.5 μA, because the amplifier's gain and output

current decrease faster than the available voltage swing over the MOSFET resistor. If the amplifier had the correct gain of two, these values would again be four times larger, around $100\,\mu A$.

If this amplifier is used in the charge-pumped biquad like the one described in sec. 7.4.2, it will dominate the THD for part of the tuning range. Its measured noise is white and scales less with tuning than the amplifier gain. If it is used to build a filter with $f_p = 4\,MHz$ and a $q_p = 3$, the resulting biquad has an SNR of 55 dB or above. Thus introducing tunable pole Qs with this current amplifier reduces the pole frequency of a filter with $q_p = 3$ from 36 MHz to 9 MHz, or by a factor of 4, if the power consumption remains the same.

Application in filters

Biquad with tunable pole frequency and pole Q — Problems with the pads

7.4.5

Finally, our second chip also contained a biquad with tunable f_p and tunable q_p. Simulations showed that it performed as would be expected, but it did not work on the chip. The reason was that we used the analogue pads provided by AMS, which have protection diodes from every pad to the negative supply *and* to the positive supply. Since the control voltage of the MOSFET resistors was set through a pad, the protection diode from the positive rail to the control pad started to conduct current, which made it impossible to set a tuning voltage higher than 3.8 V, which is still 0.2 V below the lower limit of the usable tuning range.

Pad problems

We did not notice this problem before we started our measurements, for two reasons. First, we did not expect it, since the pads we studied before were RF pads that had protection diodes only towards the negative rail. Second, the design kit supplied by AMS had a bug that made it impossible to simulate the circuits including the pads. Again, it becomes apparent how important the combination of experience and good tools is for analogue IC design.

Why we noticed the problems too late

Actually, both the charge-pumped biquad and the 7th-order filter have the same problem. However, *all* internal connections to the positive rail are made through cascode transistors like

How the problem was solved for the other circuits

the one shown in Fig. 6.4. Thus it was possible to increase the
supply voltage of the chip from 3.3 V to 5.3 V for making the
measurements, while keeping analogue ground 1.65 V above
the negative rail. This scarcely affects the properties of the
circuits, since the additional 2 V are just added to the V_{ds} of
the main transistors of the constant current sources. This was
confirmed by measurements made with the V–I converter,
which operates correctly with a 3.3 V supply.

Part III

Conclusion

Chapter 8

Comparisons and trade-offs

**If we knew what it was we were doing,
it would not be called research, would it?**

(Albert Einstein)

In this chapter, we briefly compare our filters to other filters in the literature, and then discuss several trade-offs encountered in the design of MOSFET–C SABs. The comparison part will make it apparent what kind of performance can be expected from the filters as we built them, and the trade-off section discusses various ways to change the filter performance fundamentally.

1	Sec. 7.3.3	10	[Rao99]	19	[Punzenberger98]
2	[Dehaene97]	11	[Gopinathan99]	20	[Serdijn97]
3	Sec. 7.4.3	12	[Brown99]	21	[Nagari98]
4	[Yoo98]	13	[Wu96]	22	[Helfenstein97]
5	[Celma99]	14	[Rezzi97]	23	[Huang97]
6	[Kosunen98]	15	[Tawfik87]	24	[Zele96]
7	[Mehr97]	16	[Punzenberger97]	25	[Helfenstein97]
8	[Gopinathan90]	17	[Pavan00]	26	[Chang97]
9	Sec. 7.4.2	18	[Hung97]		

Table 8.1   *References to the filters in Fig. 8.1.*

8.1   Background

When I started my scientific research, I still believed that I was expected to deliver objective results that are speaking for themselves, meaning figures. I soon found out that this is neither really possible nor a good idea, since figures are always open to interpretation.

The advice to write the evaluation of my thesis in two parts came from *Willy Sansen*, in a personal discussion at the AACD '99 in Nice. He suggested that I compare my circuits to other circuits and also tell the reader what I can achieve when I push my circuits to the limits. The second part was some problem for me, since I had neither the time nor the experience (meaning enough experienced people to talk to) to go to the limits of the feasible. The solution to my dilemma emerged in a discussion with Chris Toumazou at the ISCAS 2000, where he briefly talked about design trade-offs at a meeting I attended to. Thus the idea to give the reader some tools for sounding frontiers was born that lead me to writing the second part of this chapter.
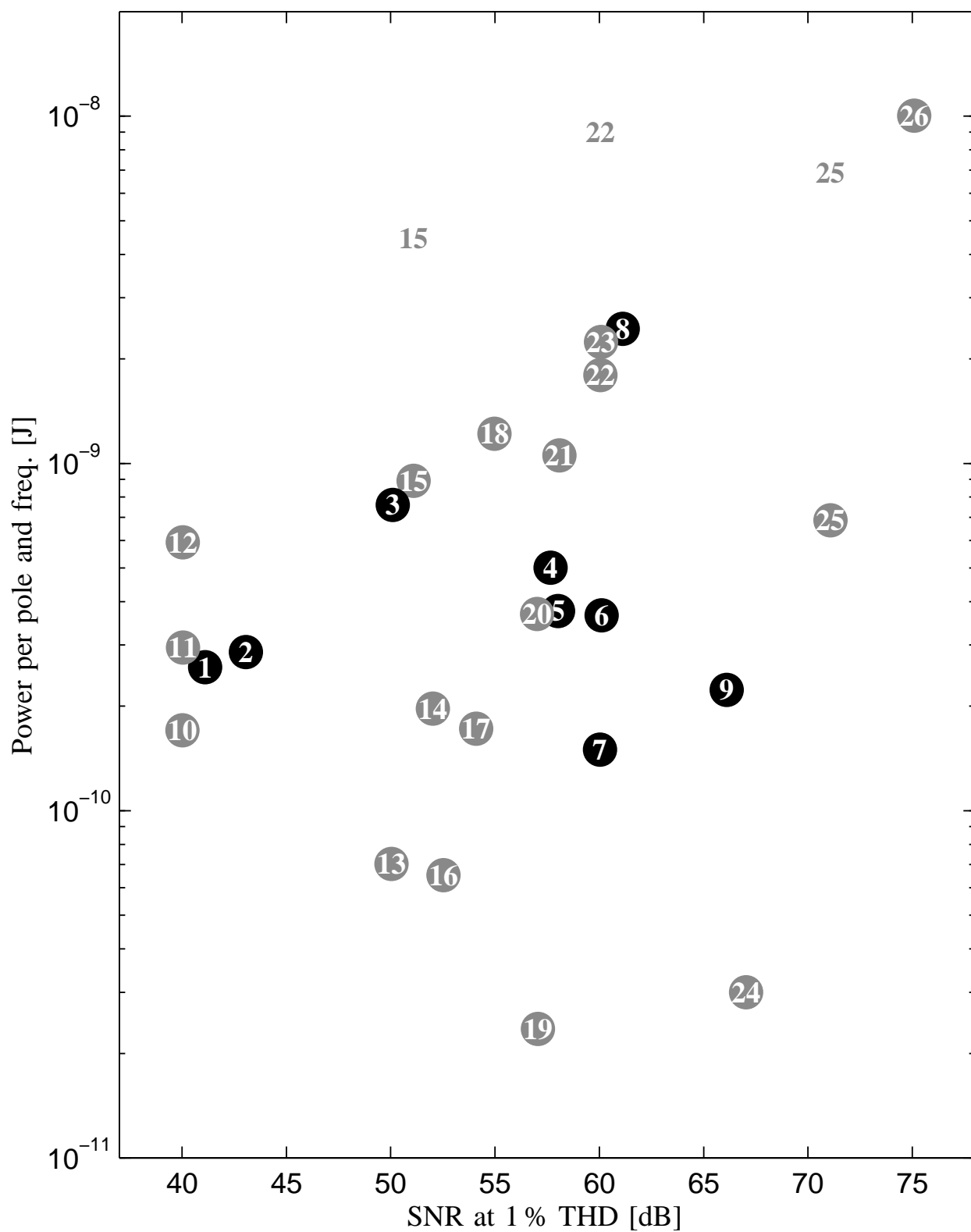
Figure of Merit for different filters in the literature. **Figure 8.1**

8.2   Comparison by figure of merit

A typical
figure of merit

A figure of merit that is often used to compare filters is the power per pole and frequency as a function of the SNR at 1 % THD. Figure 8.1 shows this figure of merit for several filters published recently; Tab. 8.1 gives the references to where each filter can be found. The black circles denote the three filters measured in this PhD thesis and six other CMOS filters from the frequency range 5–50 MHz, all of the latter are Gm–C filters. The grey circles are different filters. Note that Filters 15 and 25 are switched-capacitor filters, and Filter 22 is a switched-current filter. There are two entries for each of the switched filters, the gray number denotes the figure of merit for the pole frequency, and the gray circle stands for the sampling frequency. We included the three switched filters only to illustrate the well-known fact that switching costs power, and that the power per pole and sampling frequency of switched filters is comparable to the power per pole and frequency of continuous-time filters.

Outliers

Several things can be seen in Figure 8.1, e.g., that two filters, 19 and 24, lie far below the rest. Filter 19 is a BiCMOS log-domain filter, and Filter 24 uses positive feedback. Both filters operate around 0.5 MHz.

Biquad without
charge pump

We will now concentrate on discussing our filters and the filters that are comparable to them (the black circles). As we showed in Sec. 7.3.3, Filter 1 cannot reach high SNRs. It would, however, be suitable for building pulse equalisers similar to Filter 2. The comparison is not really fair, because Filter 2 is a 7th-order filter. We believe, however, that if an experienced analogue-IC designer used MOSFET–C biquads to build a pulse equaliser, its performance would be similar to the performance of Filter 2.

7th-order filter with
charge pump

This raises the question of biquad cascading. Filter 3 has a comparatively low dynamic range since every biquad has a low-frequency gain of two. If a gain of one was used, the maximum current through the filter would increase by a factor of about 5, the power consumption would decrease slightly, and Filter 3 would end up somewhere between Filter 6 and Filter 9. However, using unity gain would also increase the variance of the q_p of the biquadratic stages. As a compromise,

giving the highest-q_p biquad a gain of two and the remaining biquads a gain of one results in sufficiently stable poles, and places Filter 3 into the group of Filters 4, 5, and 6. Compared to these three filters, the main disadvantage of our filter is that it needs a charge pump, the main advantage is its size: it only uses $0.04\,\text{mm}^2$ per pole (including the charge pump), whereas Filter 4 (an LC ladder simulation) uses $0.25\,\text{mm}^2$ per pole, and Filter 7 uses $0.12\,\text{mm}^2$ per pole, but uses less power per pole and frequency.

Filter 9 is the best we could do with the MOSFET–C SAB technique. With its high SNR, its low power per pole and frequency, its tuning range of 26–36 MHz, and its chip area use of only $0.055\,\text{mm}^2$ per pole (including the charge pump), it is among the best available continuous-time biquadratic filter sections, at least according to the figure of merit discussed here. It is, however, an open (and complex) question how such biquads can be cascaded in an optimum way, and which performance can be achieved. The educated guess made in the previous paragraph lets one expect that it is possible to build a 7th-order Bessel filter with a power per pole and frequency of 400 pJ, an SNR at 1 % THD of 60...65 dB, and a chip area of $0.04\,\text{mm}^2$ per pole.

Charge-pumped biquad

It is of course open to debate whether a comparison by a simple figure of merit is meaningful at all. If it is, we have shown that our filters can achieve a performance similar to the performance of typical Gm–C video-frequency filters while using far less chip area. We think, however, that a figure like Fig. 8.1 should mainly be used as a map showing with which other filters one should compare ones own filters in more detail. Much more important than a comparison with other filters is a discussion of trade-offs.

Is this figure of merit meaningful?

8.3   Trade-offs

Outline

Several trade-offs that are important during the design of our filters were already discussed in various places throughout this PhD dissertation. This section covers several important trade-offs from a wider perspective; the aim is to give the reader an impression of what can or cannot be done with MOSFET–C single-amplifier SABs.

8.3.1   Local feedback and pole-Q stability

Amplifier feedback is not necessary in low-Q filters

It was shown in Sec. 3.4.2 that feedback around high-gain amplifiers or local feedback in low-gain amplifiers essentially reduces the maximum achievable pole frequency (with the exception discussed in Sec. 8.3.2). With MOSFET–C filters, such feedback also has little influence on the harmonic distortion of the filter, since this distortion comes from signal clipping caused by a saturating output stage or MOSFET resistor. Thus the main reason why one could want to use local feedback in amplifiers would be to stabilise the gain, which would reduce the variance of the pole Q. Note, however, that the variances of the component ratios also contribute to the variance of the pole Q (c.f. Sec. 4.3), so there is a limit to how much the pole-Q variance can be reduced. Furthermore, for low-Q filters ($q_p < 5$) like the one from Sec. 7.3.3, the pole-Q variance will be small enough such that using feedback techniques is not necessary.

8.3.2   Input resistance and output capacitance

Increasing the bias current

As described in Sec. 4.4, the maximum achievable pole frequency of an SAB is determined by the stopband attenuation, the input resistance of the amplifier, and its output capacitance. Since the output capacitance cannot be decreased much without reducing the voltage swing (and with it the signal swing), the only viable alternative is to reduce the input resistance. One way to do this is to simply increase the supply current of the current amplifier input stage (c.f. Fig. 6.2). However, since this current is mirrored to all other stages, increasing the supply

current makes it necessary to enlarge the current mirrors, which again increases the output capacitance, which limits the use of this method.

Another idea is to reduce the input resistance by using local feedback with a very high unity-gain bandwidth. Then the local feedback amplifier would consume the major part of the total power, which is possibly the only way to increase the maximum pole frequency considerably by trading off power efficiency.

Very fast local feedback

Maximum pole frequency and pole-Q variance   8.3.3

Another way to increase the pole frequency achievable with a certain amplifier is to decrease the spread of the passive components in the MOSFET–C SAB (c.f. Sec. 4.4). In most cases, however, doing this increases the variance of the pole Q (c.f. Sec. 4.3). In our filters, the component spreads are already very small, so only the opposite would be possible: to reduce the pole-Q variance by increasing the component spread and therefore decreasing the maximum possible pole frequency or the stop-band attenuation.

Reducing the component spreads

Signal swing, THD, and SNR   8.3.4

It was shown in Sec. 5.5.1 how the signal swing in charge-pumped MOSFET–C SABs should be set in order to maximise the SNR of the filter at a certain level of THD. However, there is little correlation between the level of THD and the SNR in a certain filter. As can be seen in Fig. 5.11, the THD curves rise very quickly because the THD is caused by clipping, so the SNR for $-40\,\mathrm{dB}$ THD would normally be only $2\,\mathrm{dB}$ larger than for $-60\,\mathrm{dB}$ THD.

THD and SNR are almost orthogonal

Cascadability and pole-Q variance   8.3.5

In order to maximise the SNR of a biquad cascade, the gains of the individual biquads should be set to unity to make the signal levels in all biquads equal. This will, however, increase the

Unity gain biquads

variance of the pole Q considerably compared to the pole-Q variance of an optimum design (c.f. 4.3).

8.3.6   Charge-pump or not?

Use a charge pump if possible

Finally, as has become apparent in Chap. 7, the advantages of having a charge-pump to drive the MOSFET resistor gates are so great that it should be done if possible. Also, the clock feed-through to the output of our filters is small enough for most applications. There are two things that could prevent the use of a charge pump.

Clock feed-through to other circuits

First, although our filters reject the substrate noise generated by the charge pump quite well, it must be made sure that the same is true for all other signal processing circuits on the chip. This may be a problem on purely analogue ICs, but is not really an issue on mixed-signal ICs, since there the substrate noise of the digital part dominates anyway.

Breakdown voltages

Second, the charge pump described in Sec. 5.5.2 is constructed so that although its output voltage can reach 5 V, no terminal voltage difference on any elements will exceed 3.3 V. Theoretically no break-down will occur even if the process used does not support 5 V as the 0.6-μm CMOS process by AMS does. The same is true for the MOSFET–C SABs. However, over-peaking during the transients might change this, and it must be made sure, by careful simulations, that the charge pump is compatible with the process at hand.

8.4   Conclusion

MOSFET–C filters are useful for video-frequency applications

We have shown in this dissertation that MOSFET–C SABs and filter cascades are a useful technique to build video-frequency filters. Their main benefit is that they require less chip area than conventional Gm–C filters having the same THD, SNR, and power consumption, typically the reduction is to 30...15 % of the size of the Gm–C filter. Since this PhD dissertation is, to our knowledge, the first comprehensive discussion of MOSFET–C SABs, many open questions still remain, which will be discussed in the following chapter.

Chapter 9

Ideas for future research

"Have you got an answer?"
"No, but I've got a different name for the problem."

(Douglas Adams)

As a conclusion of this thesis, we briefly discuss a few open questions and ideas for future research. They are mainly written for the benefit of the reader who wishes to apply MOSFET–C SABs, but also a list of directions in which the author's future research might go.

<div style="text-align: right">Outline</div>

We have given plausible arguments, based on clock feed-through measurements, for the suitability of our filters for mixed analogue-digital (MAD) IC design. The reasons for this suitability is mainly the (theoretically) perfect balancing of the circuits. To be certain, however, this suitability has to be demonstrated by actually designing a MAD IC with a MOSFET–C SAB on it, or by a detailed discussion of the substrate-noise rejection and control-signal-noise rejection of our filters.

<div style="text-align: right">Suitability for
MAD design</div>

In Chapter 2, we did not tell how a designer should actually choose the best amplifier for a certain application. This is always a difficult question, mainly because the definition of 'best' is very application specific. Also, the selection criterion for a designer is not which amplifier could be better from a theoretical point of view, but with which amplifier he personally can achieve better results. This is most probably the amplifier he is most familiar with. Thus, if the new and less well known amplifiers discussed in Chap. 2 should become viable candidates for applications, they must first be researched

<div style="text-align: right">Amplifier Choice</div>

as extensively as the well-known opamps, CFB opamps, and OTAs, such that a designer has access to the same kind of experience-based knowledge for all amplifier types.

A better variable-gain amplifier

The variable-gain current amplifier presented in Sec. 6.4 works, but it is not as well developed as the fixed-gain amplifier in Sec. 6.3. Other varieties of the concept shown in Fig.6.6 should be tried out. Two specific points at which future research should look are how the voltage buffers driving the MOSFET resistor may be improved, and whether the whole chain of current buffer, poly-silicon resistor, and voltage buffer could be replaced by a resistor-less transresistance amplifier.

Ceteris paribus comparison

The current-mode vs. voltage-mode debate is still open, so it would be interesting to have a ceteris paribus comparison, an example of two filters that are as similar as possible and differ only in the mode of the signal. We have very good reasons to believe that these two filters would then perform equally well (c.f. Chap. 3), but it would be nice to have a more conclusive proof or refutation.

Bandpass filters

All filters built for this thesis were low-pass filters, i.e., filters that may be used for anti-aliasing or for pulse shaping. The design decisions for building bandpass filters will be different, and the discussion of harmonic distortion has to be extended to a discussion of inter-modulation distortion.

Detailed discussion of MOSFET-only SABs

We have shown by simulations that our filters can also be built as MOSFET-only filters if gate capacitors instead of signal capacitors are used. This would make our filters suitable for standard digital CMOS processes. However, the optimum choice of the analogue ground as well as the signal swing that optimises the SNR will have to be re-evaluated, and some research must be done on which kind of MOSFET capacitor to use and, if it lies in its own well, how to bias its well.

Higher-order single-amplifier filters

It was briefly mentioned in Chap. 5 that one can also build third-order or even higher-order filters with just one amplifier. We think that this would work too, but that the performance would not be considerably better than for MOSFET–C SABs, mainly because amplifier non-idealities cause worse problems for higher-order filters. In order to find out whether this is indeed so, many of the discussions in this thesis have to be extended to third-order single-amplifier filters, which is a

difficult task that does not promise closed-form results, because of the far greater complexity of the symbolic formulation of third-order transfer functions.

The biquad cascade presented in Sec. 7.4.3 can certainly be improved, but in order to optimise it for maximum SNR, similar principles that are used for the optimisation of discrete-component filter cascades must be adapted for MOSFET–C SABs.

<div style="text-align:right">Optimum
Biquad Cascades</div>

The SNR of a MOSFET–C filter can be improved if its tuning range is reduced. If the continuous tuning should cover the whole range necessary to compensate fabrication differences, the tuning voltage range must be comparatively wide. An alternative would be to tune the filter coarsely in steps, by switching capacitors on and off, and to do only the fine-tuning with the MOSFET resistors. It is not clear by how much such a procedure could increase the SNR, but it would make it possible to build better charge-pump-less filters.

<div style="text-align:right">Discontinuous tuning</div>

Finally, we cannot yet tell how good the yield of our filters is. We only got 15 samples back from each chip, in each case, the yield was 100 %. (We destroyed one sample of chip 1 by tearing off a few bonding wires while inexpertly removing the lid with a pen knife to make a chip photo.) Since our filters are low-Q filters based on robust circuits, we expect a high yield, the main problems could be caused by the charge pump. A reliable statement about the yield would, however, require the production of a much higher number of samples than we could afford.

<div style="text-align:right">Yield</div>

Glossary

ASF Analoge Signalverarbeitung und Filterung;
a lecture series at ETH Zürich

CCII Second-generation current conveyor

CFB (opamp/OTA) Current-feedback (opamp/OTA)

CMOS (process) Complementary
metal-oxide-semiconductor (process)

DDOA Differential-difference opamp

DP SFG Driving-point signal-flow graph

FDNR Frequency-dependent negative resistor;
has the Impedance $Z = 1/D s^2$

Gm–C filter Filter containing integrators that are composed
of OTAs and capacitors

MOSFET Metal-oxide-semiconductor field-effect transistor

MOSFET–C filter RC filter with all resistors replaced
by MOSFETs operating in the triode region

OFA Operational floating amplifier, or floating opamp

OFC Operational floating conveyor

opamp Operational amplifier

OTA Operational transconductance amplifier

OTRA Operational transresistance amplifier

RLC filter Filter containing resistors, inductors,
and capacitors

SAB Single-amplifier biquadratic filter

SFDR Spurious-free dynamic range

SFG Signal-flow graph

VICCII Voltage-inverting second-generation current conveyor

Bibliography

Phillip E. Allen, Benjamin J. Blalock, and Stephen Stephen W. Milam. "Low-gain active filters." In *The Circuits and Filters Handbook* (edited by Wai-Kai Chen), chap. 75, pp. 2339–2371. CRC Press, Inc., Boca Raton, Florida, 1995.　　　　　　　　　　　　　[Allen95]

Analog Devices. "AD 844 data sheet." In *Analog Devices Amplifier Reference Manual*. 1992.　　　　　　　　　　　　　[Analog Devices92]

Arie F. Arbel and Lavy Goldminz. "Output stage for current-mode feedback amplifiers, theory and applications." *Analog Integrated Circuits and Signal Processing*, vol. 2, no. 3, pp. 243–255, Sep. 1992.　　　　　　　　　　　　　[Arbel92]

Arie F. Arbel. "Towards a perfect CMOS CCII." *Analog Integrated Circuits and Signal Processing*, vol. 12, pp. 119–132, 1997.　　　　　　　　　　　　　[Arbel97]

Mihai Banu and Yannis Tsividis. "Fully integrated active RC filters in MOS technology." *IEEE Journal of Solid-State Circuits*, vol. 18, no. 6, pp. 644–651, Dec. 1983.　　　　　　　　　　　　　[Banu83]

Mihai Banu and Yannis Tsividis. "Detailed analysis of nonidealities in MOS fully integrated active RC filters based on balanced networks." *IEE Proceedings, Part G*, vol. 131, no. 5, pp. 190–196, Oct. 1984.　　　　　　　　　　　　　[Banu84]

Mihai Banu and Yannis Tsividis. "An elliptic continuous-time CMOS filter with on-chip automatic tuning." *IEEE Journal of Solid-State Circuits*, vol. 20, no. 6, pp. 1114–1121, Dec. 1985.　　　　　　　　　　　　　[Banu85]

B. B. Bhattacharyya and M. N. S. Swamy. "Network transposition and its application in synthesis." *IEEE Transactions on Circuit Theory*, vol. CT-18, no. 3, pp. 394–397, May 1971.　　　　　　　　　　　　　[Bhattacharyya71]

Derek F. Bowers. "The so-called current-feedback operational amplifier... technological breaktrough or engineering curiosity?" In *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 1054–1057. Chicago, 1993.　　　　　　　　　　　　　[Bowers93]

James E. C. Brown, Paul J. Hurst, Bret C. Rothenberg, and Stephen H. Lewis. "A CMOS adaptive continuous-time forward equalizer, LPF, and RAM-DFE for magnetic recording." *IEEE Journal of Solid-State Circuits*, vol. 34, no. 2, pp. 162–169, Feb. 1999.　　　　　　　　　　　　　[Brown99]

[Bruun93]   Erik Bruun. "CMOS technology and current-feedback op-amps." In *Proceedings of the IEEE International Symposium on Circuits and Systems*, vol. 2, pp. 1062–1065. Chicago, 1993.

[Bruun95]   Erik Bruun. "Class AB CMOS first-generation current conveyor." *Electronics Letters*, vol. 31, no. 6, pp. 422–423, Mar. 1995.

[Bruun98]   Erik Bruun. "Worst case estimate of mismatch induced distortion in complementary CMOS current mirrors." *Electronics Letters*, vol. 34, no. 17, pp. 1625–1627, Aug. 1998.

[Bruun99]   Erik Bruun. "Analytical expressions for harmonic distortion at low frequencies due to device mismatch in CMOS current mirrors." *IEEE Transactions on Circuits and Systems–II: Analog and Digital Signal Processing*, vol. 46, no. 7, pp. 937–941, Jul. 1999.

[Bucher96a] Matthias Bucher, Christophe Lallement, and Christian C. Enz. "An efficient parameter extraction methodology for the EKV MOST model." In *Proceedings of the IEEE International Conference on Microelectronic Test Structures*, pp. 145–150. Trento, Italy, 1996.

[Bucher96b] Matthias Bucher, Christophe Lallement, Christian C. Enz, and François Krummenacher. "Accurate MOS modelling for analog circuit simulation using the EKV model." In *Proceedings of the IEEE International Symposium on Circuits and Systems*, vol. 4, pp. 703–706. Atlanta, 1996.

[Burger96]   Thomas Burger and Qiuting Huang. "A 100 dB, 480 MHz OTA in 0.7 μm CMOS for sampled-data applications." In *Proceedings of the IEEE Custom Integrated Circuit Conference*, pp. 101–104. San Diego, California, May 1996.

[Burr Brown95] Burr Brown. "OPA 660 data sheet." In *Burr Brown IC Data Book — Linear Products*. 1995.

[Cabeza94]   Rafael Cabeza, Alfonso Carlosena, and Luis Serrano. "Unified approach to the implementation of universal active devices." *Electronics Letters*, vol. 30, no. 8, pp. 618–620, Apr. 1994.

[Cabeza97]   Rafael Cabeza and Alfonso Carlosena. "Analog universal active device: theory, design and applications." *Analog Integrated Circuits and Signal Processing*, vol. 12, no. 2, pp. 153–168, Feb. 1997.

[Carlin64]   Herbert J. Carlin. "Singular network elements." *IEEE Transactions on Circuit Theory*, vol. 11, no. 1, pp. 67–72, Mar. 1964.

[Carlosena92] Alfonso Carlosena, Sonia Porta, and George S. Moschytz. "Current-mode realization of negative feedback SAB's." In *35th Midwest Symposium on Circuits and Systems*, pp. 1296–1299. Washington, Aug. 1992.

Alfonso Carlosena and George S. Moschytz. "Nullators and no-   [Carlosena93]
rators in voltage to current mode transformations." *International
Journal on Circuit Theory and Applications*, vol. 21, no. 4, pp.
421–424, Jul. 1993.

Alfonso Carlosena, Rafael Cabeza, and Luis Serrano. "On the   [Carlosena94]
search for a "universal" active element." In *Proceedings of the
IEEE International Symposium on Circuits and Systems*, vol. 5, pp.
779–782. London, Jun. 1994.

S. Celma, J. Sabadell, C. Aldea, and P. A. Martínez. "Video-   [Celma99]
frequency current-voltage mode integrator." *Electronics Letters*,
vol. 35, no. 10, pp. 773–775, May 1999.

Zhong Yuan Chang, D. Haspeslagh, and J. Verfaillie. "A highly   [Chang97]
linear CMOS G_m-C bandpass filter with on-chip frequency tuning."
IEEE Journal of Solid-State Circuits, vol. 32, no. 3, pp. 388–397,
Mar. 1997.

Ray R. Chen, Artice M. Davis, and Marwan A. Simaan. "Network   [Chen95]
laws and theorems." In *The Circuits and Filters Handbook* (edited
by Wai-Kai Chen), chap. 13, pp. 418–474. CRC Press, Inc., Boca
Raton, Florida, 1995.

W. Chiu, S.-I. Liu, H.-W. Tsao, and J.-J. Chen. "CMOS differ-   [Chiu96]
ential difference current conveyors and their applications." *IEE
Proceedings – Circuits, Devices and Systems*, vol. 143, no. 2, pp.
91–96, Apr. 1996.

Zdzislaw Czarnul. "Novel MOS resistive circuit for synthesis of   [Czarnul86]
fully integrated continuous-time filters." *IEEE Transactions on
Circuits and Systems*, vol. 33, no. 7, pp. 718–721, Jul. 1986.

Zdzislaw Czarnul and Yannis P. Tsividis. "Implementation of   [Czarnul88]
MOSFET-C filters based on active RC prototypes." *Electronics
Letters*, vol. 24, no. 3, pp. 184–185, Feb. 1988.

Wim Dehaene, Michiel S. J. Steyaert, and Willy Sansen. "A 50-   [Dehaene97]
MHz standard CMOS pulse equalizer for hard disk read channels."
IEEE Journal of Solid-State Circuits, vol. 32, no. 7, pp. 977–988,
Jul. 1997.

Stephen W. Director and Ronald A. Rohrer. "The generalized   [Director69]
adjoint network and network sensitivities." *IEEE Transactions on
Circuit Theory*, vol. 16, no. 3, pp. 318–323, Aug. 1969.

Tonny A. F. Duisters and Eise Carel Dijkmans. "A −90-dB THD   [Duisters98]
rail-to-rail input opamp using a new local charge pump in CMOS."
IEEE Journal of Solid-State Circuits, vol. 33, no. 7, pp. 947–955,
Jul. 1998.

Christian C. Enz, François Krummenacher, and Eric A. Vittoz.   [Enz95]
"An analytical MOS transistor model valid in all regions of oper-

ation and dedicated to low-voltage and low-current applications." *Analog Integrated Circuits and Signal Processing*, vol. 8, no. 1, pp. 83–114, Jul. 1995.

[Espley33]   D. C. Espley.   "The calculation of harmonic production in thermionic valves with resistive loads." *Proceedings of the Institute of Radio Engineers*, vol. 21, no. 10, pp. 1439–1446, Oct. 1933.

[Fabre95]   Alain Fabre.   "Third-generation current conveyor: a new helpful active element." *Electronics Letters*, vol. 31, no. 5, pp. 338–339, Mar. 1995.

[Franco93]   Sergio Franco.   "Analytical foundations of current feedback amplifiers." In *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 1050–1053. Chicago, 1993.

[Gopinathan90]   Venugopal Gopinathan, Yannis Tsividis, Khen-Sang Tan, and Richard Hester.   "A 5V 7th-order elliptic analog filter for digital video applications." In *Proceedings of the IEEE International Solid-State Circuits Conference*, pp. 208–209. San Francisco, Feb. 1990.

[Gopinathan99]   Venu Gopinathan, Maurice Tarsia, and Davy Choi.   "Design considerations and implementation of a programmable high-frequency continuous-time filter and variable-gain amplifier in submicrometer CMOS." *IEEE Journal of Solid-State Circuits*, vol. 34, no. 12, pp. 1698–1707, Dec. 1999.

[Harvey93]   Barry Harvey.   "Current feedback opamp limitations: A state-of-the-art review." In *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 1066–1069. Chicago, 1993.

[Hasler95]   Martin Hasler.   "Nonlinear circuits: Qualitative analysis."   In *The Circuits and Filters Handbook* (edited by Wai-Kai Chen), chap. 31, pp. 914–934. CRC Press, Inc., Boca Raton, Florida, 1995.

[Hassoun95]   Marwan M. Hassoun.   "Computer-aided design and optimization: Symbolic analysis methods." In *The Circuits and Filters Handbook* (edited by Wai-Kai Chen), chap. 52, pp. 1392–1411. CRC Press, Inc., Boca Raton, Florida, 1995.

[Helfenstein97]   Markus Helfenstein. *Analysis and Design of Switched-Current Networks*.   Ph.D. thesis, Swiss Federal Institute of Technology (ETH), Zürich, Switzerland, 1997. (Diss. ETH No. 12257).

[Horowitz89]   Paul Horowitz and Winfield Hill. *The Art of Electronics*.   Cambridge University Press, second edn., 1989. ISBN 0-521-37095-7.

[Huang97]   Qiuting Huang.   "A MOSFET-only continuous-time bandpass filter." *IEEE Journal of Solid-State Circuits*, vol. 32, no. 2, pp. 147–158, Feb. 1997.

Lawrence P. Huelsman and Phillip E. Allen. *Introduction to the theory and design of active filters*. McGraw-Hill Book Company, New York, 1980. ISBN 0-07-030854-3.   [Huelsman80]

Johan H. Huijsing and Jacob De Korte. "Monolithic nullor — a universal active network element." *IEEE Journal of Solid-State Circuits*, vol. 12, no. 1, pp. 59–64, Feb. 1977.   [Huijsing77]

Johan H. Huijsing. "Operational floating amplifier." *IEE Proceedings, Part G*, vol. 137, no. 2, pp. 131–136, Apr. 1990.   [Huijsing90]

Chung-Chih Hung, Kari A. I. Halonen, Mohammed Ismail, Veikko Porra, and Akira Hyogo. "A low-voltage, low-power CMOS fifth-order elliptic GM-C filter for baseband mobile, wireless communication." *IEEE Transactions on Circuits and Systems for Video Technology*, vol. 7, no. 4, pp. 584–593, Aug. 1997.   [Hung97]

David A. Johns and Ken Martin. *Analog Integrated Circuit Design*. John Wiley & Sons, New York, 1997. ISBN 0-471-14448-7.   [Johns97]

Thomas Kaulberg. "A CMOS current-mode operational amplifier." *IEEE Journal of Solid-State Circuits*, vol. 28, no. 7, pp. 849–852, Jul. 1993.   [Kaulberg93]

Chun-Sup Kim, Gea-Ok Cho, Yong-Hwan Kim, and Bang-Sup Song. "A CMOS $4\times$ speed DVD read channel IC." *IEEE Journal of Solid-State Circuits*, vol. 33, no. 8, pp. 1168–1178, Aug. 1998.   [Kim98]

Marko Kosunen, Kimmo Koli, and Kari Halonen. "A 50 MHz 5th order elliptic LP-filter using current mode gm-C topology." In *Proceedings of the IEEE International Symposium on Circuits and Systems*, vol. 1, pp. 512–515. Monterey, California, Jun. 1998.   [Kosunen98]

Tom Kwan and Kenneth Martin. "An adaptive analog continuous-time CMOS biquadratic filter." *IEEE Journal of Solid-State Circuits*, vol. 26, no. 6, pp. 859–867, Jun. 1991.   [Kwan91]

Kenneth R. Laker and Willy M. C. Sansen. *Design of analog integrated circuits and systems*. McGraw-Hill, New York, 1994. ISBN 0-07-036060-1.   [Laker94]

A. Leuciuc. "Using nullors for realisation of inverse transfer functions and characteristics." *Electronics Letters*, vol. 33, no. 11, pp. 949–951, May 1997.   [Leuciuc97]

John Lidgey, Chris Toumazou, Alison Payne, Doug C. Wadsworth, Sittichai Pookaiyaudom, and Erik Bruun. "Tutorial 10: Current-mode analog signal processing; Part 2: current conveyors." In *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 569–641. London, 1994.   [Lidgey94]

Saska Lindfors, Jarkko Jussila, Kari Halonen, and Lauri Siren. "A 3-V continuous-time filter with on-chip tuning for IS-95." *IEEE*   [Lindfors99]

Journal of Solid-State Circuits, vol. 34, no. 8, pp. 1150–1154, Aug. 1999.

[Lu94]   Ping-Hsing Lu, Chung-Yu Wu, and Ming-Kai Tsai. "Design techniques for tunable transresistance-C VHF bandpass filters." *IEEE Journal of Solid-State Circuits*, vol. 29, no. 9, pp. 1058–1067, Sep. 1994.

[Mahattanakul98] Jirayuth Mahattanakul and Chris Toumazou. "Current-mode versus voltage-mode G_m–C biquad filters: What the theory says." *IEEE Transactions on Circuits and Systems–II: Analog and Digital Signal Processing*, vol. 45, no. 2, pp. 173–186, Feb. 1998.

[Mason53]   Samuel J. Mason. "Feedback theory — Some properties of signal flow graphs." *Proceedings of the Institute of Radio Engineers*, vol. 41, no. 9, pp. 1144–1156, Sep. 1953.

[Mason56]   Samuel J. Mason. "Feedback theory — Further properties of signal flow graphs." *Proceedings of the Institute of Radio Engineers*, vol. 44, no. 7, pp. 920–926, Jul. 1956.

[Mehr97]   Iuri Mehr and David R. Welland. "A CMOS continuous-time G_m–C filter for PRML read channel applications at 150 Mb/s and beyond." *IEEE Journal of Solid-State Circuits*, vol. 32, no. 4, pp. 499–513, Apr. 1997.

[Moschytz74]   George S. Moschytz. *Linear Integrated Networks: Fundamentals.* Bell Laboratories Series. Van Nostrand Reinhold, New York, 1974. ISBN 0-442-25581-0.

[Moschytz75]   George S. Moschytz. *Linear Integrated Networks: Design.* Bell Laboratories Series. Van Nostrand Reinhold, New York, 1975.

[Moschytz80]   George S. Moschytz. "Single-amplifier active filters: A review." *Scientia Electrica*, vol. 26, no. 1, pp. 1–46, 1980.

[Moschytz81]   George S. Moschytz and P. Horn. *Active filter design handbook.* John Wiley & Sons, Chichester, 1981. ISBN 0-471-27850-5.

[Moschytz94]   George S. Moschytz and A. Carlosena. "A classification of current-mode single-amplifier biquads based on a voltage-to-current transformation." *IEEE Transactions on Circuits and Systems–II: Analog and Digital Signal Processing*, vol. 41, no. 2, pp. 151–156, Feb. 1994.

[Moschytz99a]   George S. Moschytz. "Low-sensitivity, low-power active-RC allpole filters using impedance tapering." *IEEE Transactions on Circuits and Systems–II: Analog and Digital Signal Processing*, vol. 46, no. 8, pp. 1009–1026, Aug. 1999.

[Moschytz99b]   George S. Moschytz. "Realizability constraints for third-order impedance-tapered allpole filters." *IEEE Transactions on Circuits*

and Systems–II: Analog and Digital Signal Processing, vol. 46, no. 8, pp. 1073–1077, Aug. 1999.

Igor Mucha. "Current operational amplifiers: basic architecture, properties, exploitation and future." *Analog Integrated Circuits and Signal Processing*, vol. 7, no. 3, pp. 243–255, May 1995.   [Mucha95]

Igor Mucha. "Low-voltage current operational amplifier with a very low current consumption." In *Proceedings of the IEEE International Symposium on Circuits and Systems*, vol. 1, pp. 525–528. Atlanta, 1996.   [Mucha96]

Angelo Nagari and Germano Nicollini. "A 3 V 10 MHz pseudo-differential SC bandpass filter using gain enhancement replica amplifier." *IEEE Journal of Solid-State Circuits*, vol. 33, no. 4, pp. 626–630, Apr. 1998.   [Nagari98]

Bram Nauta. "A CMOS transconductance-C filter technique for very high frequencies." *IEEE Journal of Solid-State Circuits*, vol. 27, no. 2, pp. 142–153, Feb. 1992.   [Nauta92]

Agustin Ochoa. "A systematic approach to the analysis of general and feedback circuits and systems using signal flow graphs and driving-point impedance." *IEEE Transactions on Circuits and Systems–II: Analog and Digital Signal Processing*, vol. 45, no. 2, pp. 187–195, Feb. 1998.   [Ochoa98]

Giuseppe Palmisano, Gaetano Palumbo, and Salvatore Pennisi. "A CMOS transresistance current amplifier." In *Proceedings of the IEEE International Symposium on Circuits and Systems*, vol. 3, pp. 1960–1963. Hong Kong, 1997.   [Palmisano97]

Giuseppe Palmisano and Gaetano Palumbo. "High-drive CMOS current amplifier." *IEEE Journal of Solid-State Circuits*, vol. 33, no. 2, pp. 228–236, Feb. 1998.   [Palmisano98]

Shanthi Pavan, Yannis P. Tsividis, and Krishnaswamy Nagaraj. "Widely programmable high-frequency continuous-time filters in digital CMOS technology." *IEEE Journal of Solid-State Circuits*, vol. 35, no. 4, pp. 503–511, Apr. 2000.   [Pavan00]

Alison Payne and Chris Toumazou. "Operational floating conveyor." In *Proceedings of the IEEE International Symposium on Circuits and Systems*, vol. 3, pp. 1813–1816. Singapore, 1991.   [Payne91]

Alison Payne and Chris Toumazou. "Analog amplifiers: Classification and generalization." *IEEE Transactions on Circuits and Systems–I: Fundamental Theory and Applications*, vol. 43, no. 1, pp. 43–50, Jan. 1996.   [Payne96]

Manfred Punzenberger and Christian C. Enz. "A 1.2-V low-power BiCMOS class AB log-domain filter." *IEEE Journal of Solid-State Circuits*, vol. 32, no. 12, pp. 1968–1978, Dec. 1997.   [Punzenberger97]

[Punzenberger98] Manfred Punzenberger and Christian C. Enz. "A compact low-power BiCMOS log-domain filter." *IEEE Journal of Solid-State Circuits*, vol. 33, no. 7, pp. 1123–1129, Jul. 1998.

[Rao99] Narendra Rao, V. Balan, and R. Contreras. "A 3-V, 10–100-MHz continuous-time seventh-order 0.05° equiripple linear phase filter." *IEEE Journal of Solid-State Circuits*, vol. 34, no. 11, pp. 1676–1682, Nov. 1999.

[Rezzi97] Francesco Rezzi, Ivan Bietti, Marco Cazzaniga, and Rinaldo Castello. "A 70-mW seventh-order filter with 7–50 MHz cutoff frequency and programmable boost and group delay equalization." *IEEE Journal of Solid-State Circuits*, vol. 32, no. 12, pp. 1987–1999, Dec. 1997.

[Roberts89a] Gordon W. Roberts and Adel S. Sedra. "All current-mode frequency selective circuits." *Electronics Letters*, vol. 25, no. 12, pp. 759–761, Jun. 1989.

[Roberts89b] Gordon W. Roberts and Adel S. Sedra. "A generalization of intermediate transfer function analysis to arbitrary linear networks." In *Proceedings of the IEEE International Symposium on Circuits and Systems*, vol. 2, pp. 1059–1062. Portland, Oregon, May 1989.

[Roberts90] Gordon W. Roberts. "Adjoint networks revisited." In *Proceedings of the IEEE International Symposium on Circuits and Systems*, vol. 1, pp. 540–544. New Orleans, 1990.

[Roberts92] Gordon W. Roberts and Adel S. Sedra. "A general class of current amplifier-based biquadratic filter circuits." *IEEE Transactions on Circuits and Systems–I: Fundamental Theory and Applications*, vol. 39, no. 4, pp. 257–263, Apr. 1992.

[Säckinger87] Eduard Säckinger and Walter Guggenbühl. "A versatile building block: the CMOS differential difference amplifier." *IEEE Journal of Solid-State Circuits*, vol. 22, no. 2, pp. 287–294, Apr. 1987.

[Säckinger90] Eduard Säckinger and Walter Guggenbühl. "A high-swing, high-impedance MOS cascode circuit." *IEEE Journal of Solid-State Circuits*, vol. 25, no. 1, pp. 289–298, Feb. 1990.

[Sallen55] R. P. Sallen and E. L. Key. "A practical method of designing RC active filters." *IRE Transactions on Circuit Theory*, vol. CT-2, no. 1, pp. 74–85, Mar. 1955.

[Sansen99] Willy Sansen. "Distortion in elementary transistor circuits." *IEEE Transactions on Circuits and Systems–II: Analog and Digital Signal Processing*, vol. 46, no. 3, pp. 315–325, Mar. 1999.

[Schmid97] Hanspeter Schmid and George S. Moschytz. "Tunable CCII-MOSFET-C filter biquads for video frequencies." In *Proceedings of the European Conference on Circuit Theory and Design*, vol. 1, pp. 82–87. Budapest, 1997.

Hanspeter Schmid. "The ideal amplifier myth, and a complete am-   [Schmid98a]
plifier classification." Tech. Rep. 9801, Swiss Federal Institute of
Technology, Signal and Information Processing Laboratory, Zürich,
Switzerland, Jan. 1998.

Hanspeter Schmid. "Understanding integrated amplifiers." Tech.   [Schmid98b]
Rep. 9802, Swiss Federal Institute of Technology, Signal and In-
formation Processing Laboratory, Zürich, Switzerland, Mar. 1998.

Hanspeter Schmid and George S. Moschytz. "Fundamental fre-   [Schmid98c]
quency limitations in current-mode Sallen-Key filters." In *Pro-
ceedings of the IEEE International Symposium on Circuits and
Systems*, vol. 1, pp. 57–60. Monterey, California, Jun. 1998.

Hanspeter Schmid and George S. Moschytz. "A continuously   [Schmid99a]
adjustable video-frequency current amplifier for filter applications."
In *Proceedings of the European Conference on Circuit Theory and
Design*, vol. 1, pp. 305–309. Stresa, Italy, Aug. 1999.

Hanspeter Schmid and George S. Moschytz. "A tunable, video-   [Schmid99b]
frequency, low-power, single-amplifier biquadratic filter in CMOS."
In *Proceedings of the IEEE International Symposium on Circuits
and Systems*, vol. 2, pp. 128–131. Orlando, Florida, Jun. 1999.

Hanspeter Schmid. "Black tools — how to win a debate." *IEEE   [Schmid00a]
Professional Communication Society Newsletter*, vol. 43–44, no.
2/1999–2/2000, 1999–2000. Appeared in seven parts.

Hanspeter Schmid. "Approximating the universal active element."   [Schmid00b]
*IEEE Transactions on Circuits and Systems–II: Analog and Digital
Signal Processing*, 2000. Accepted for publication in the Novem-
ber 2000 issue.

Hanspeter Schmid and George S. Moschytz. "A 8.25-MHz 7th-   [Schmid00c]
order Bessel filter built with MOSFET–C single-amplifier biquads."
In *Proceedings of the NORCHIP*. Turku, Finland, Nov. 2000. (ac-
cepted for publication).

Hanspeter Schmid and George S. Moschytz. "Active-MOSFET-   [Schmid00d]
C single-amplifier biquadratic filters for video frequencies." *IEE
Proceedings – Circuits, Devices and Systems*, vol. 147, no. 1, pp.
35–41, Feb. 2000.

Hanspeter Schmid and George S. Moschytz. "A charge-pump-   [Schmid00e]
controlled MOSFET–C single-amplifier biquad." In *Proceedings of
the IEEE International Symposium on Circuits and Systems*, vol. 2,
pp. 677–680. Geneva, Switzerland, May 2000.

A. S. Sedra and K. C. Smith. "A second generation current con-   [Sedra70]
veyor and its applications." *IEEE Transactions on Circuit Theory*,
vol. 17, no. 1, pp. 132–134, Feb. 1970.

[Sedra90]   A. S. Sedra, G. W. Roberts, and F. Gohh. "The current conveyor: history, progress and new results." *IEE Proceedings, Part G*, vol. 137, no. 2, pp. 78–87, Apr. 1990.

[Serdijn97]   Wouter A. Serdijn, Martijn Broest, Jan Mulder, Albert C. van der Woerd, and Arthur H. M. van Roermund. "A low-voltage ultra-low-power translinear integrator for audio filter applications." *IEEE Journal of Solid-State Circuits*, vol. 32, no. 4, pp. 577–581, Apr. 1997.

[Smith68]   K. C. Smith and A. S. Sedra. "The current conveyor — a new circuit building block." *Proceedings of the IEEE*, vol. 56, no. 8, pp. 1368–1369, Aug. 1968.

[Svoboda91]   James A. Svoboda, L. McGory, and S. Webb. "Applications of a commercially available current conveyor." *International Journal of Electronics*, vol. 70, no. 1, pp. 159–164, Jan. 1991.

[Svoboda95]   James A. Svoboda. "Using nullors to analyze linear networks." In *The Circuits and Filters Handbook* (edited by Wai-Kai Chen), chap. 22, pp. 751–775. CRC Press, Inc., Boca Raton, Florida, 1995.

[Tawfik87]   Mohamed Sameh Tawfik and Patrice Senn. "A 3.6-MHz cutoff frequency CMOS elliptic low-pass switched-capacitor ladder filter for video communication." *IEEE Journal of Solid-State Circuits*, vol. 22, no. 3, pp. 378–384, Jun. 1987.

[Tellegen54]   B. D. H. Tellegen. "La recherche pour una série complète d'éléments de circuit ideaux non-linéaires." *Rendiconti del Seminario Matematico e Fisico di Milano*, vol. 25, pp. 134–144, Apr. 1954.

[Toumazou90]   Chris Toumazou, F. J. Lidgey, and D. G. Haigh. *Analogue IC design: the current-mode approach*, vol. 2 of *IEE Circuits and Systems Series 2*. Peter Peregrinus Ltd., 1990. ISBN 0-86341-215-7.

[Toumazou93]   Chris Toumazou, Alison Payne, and John Lidgey. "Current-feedback versus voltage-feedback amplifiers: History, insight and relationships." In *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 1046–1049. Chicago, 1993.

[Tsividis86]   Yannis Tsividis, Mihai Banu, and John Khoury. "Continuous-time MOSFET-C filters in VLSI." *IEEE Journal of Solid-State Circuits*, vol. 21, no. 1, pp. 15–30, Feb. 1986.

[Tsividis93]   Y. P. Tsividis and J. O. Voorman (eds.). *Integrated Continuous-Time Filters — Principles, Design, and Applications*. IEEE Press, New York, 1993. ISBN 0-7803-0425-X.

[Tsividis96]   Yannis Tsividis. *Mixed analog-digital VLSI devices and technology*. McGraw-Hill, New York, 1996. ISBN 0-07-065402-6.

Z. Wang. "Analytical determination of output resistance and DC matching errors in MOS current mirrors." *IEE Proceedings, Part G*, vol. 137, no. 5, pp. 397–404, Oct. 1990. [Wang90]

B. Wilson. "Recent developments in current conveyors and current-mode circuits." *IEE Proceedings, Part G*, vol. 137, no. 2, pp. 63–77, Apr. 1990. [Wilson90]

B. Wilson. "Tutorial review: Trends in current conveyor and current-mode amplifier design." *International Journal of Electronics*, vol. 73, no. 3, pp. 573–583, 1992. [Wilson92]

Chung-Yu Wu and Heng-Shou Hsu. "The design of CMOS continuous-time VHF current and voltage-mode lowpass filters with Q-enhancement circuits." *IEEE Journal of Solid-State Circuits*, vol. 31, no. 5, pp. 614–624, May 1996. [Wu96]

Johan Wulleman. "A low-power high-gain transresistance BiCMOS pulse amplifier for capacitive detector readout." *IEEE Journal of Solid-State Circuits*, vol. 32, no. 8, pp. 1181–1191, Aug. 1997. [Wulleman97]

Changsik Yoo, Seung-Wook Lee, and Wonchan Kim. "A ±1.5-V, 4-MHz CMOS continuous-time filter with a single-integrator based tuning." *IEEE Journal of Solid-State Circuits*, vol. 33, no. 1, pp. 18–27, Jan. 1998. [Yoo98]

Rajesh H. Zele and David J. Allstot. "Low-power CMOS continuous-time filters." *IEEE Journal of Solid-State Circuits*, vol. 31, no. 2, pp. 157–168, Feb. 1996. [Zele96]

The author's biography

Hanspeter Schmid went to primary and secondary school in Seengen, Switzerland. In 1983 he lost both hands in an explosives accident, and had to repeat one school year to compensate for the long stay in hospital. From 1985–1988, he went to the Kantonsschule[1] Aarau, where he got his Maturität of type C [2].

He studied Electrical Engineering at the ETH[3] in Zürich, with a one-year break after the third year, during which he worked as a development engineer at Camille Bauer AG (Wohlen, Switzerland) and went to Edinburgh to study English. He received his diploma in electrical engineering in 1994 and the post-graduate degree in information technologies in 1999.

Hanspeter Schmid joined the Signal and Information Processing Laboratory of the ETH Zürich as a teaching assistant in 1994 and started his PhD studies late in 1995. After finishing this dissertation, he starts working as an analogue-IC designer for Bernafon, Switzerland, but continues being a senior lecturer in the field of analogue integrated filters at ETH Zürich. He also serves the IEEE Circuits and Systems Society as a member (currently the Secretary) of the Analog Signal Processing Committee.

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