Active-MOSFET-C single-amplifier biquadratic filters for video frequencies

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Abstract: The authors show how continuous-time active-RC filters can be implemented in CMOS by replacing all resistors by MOSFETs operating in the linear region. As an example, a 24MHz active-MOSFET-C single-amplifier biquadratic lowpass filter with a pole-Q of 3 implemented in a 0.6μm CMOS process is discussed. By comparing measurements of a test chip, simulations and calculations, the following conclusion is reached: as long as the specifications for frequency, pole-Q, spurious-free dynamic range and supply voltage lie within certain limits, then active-MOSFET-C single-amplifier biquads (MOSFET-C SABs) are preferable, with respect to chip size and power consumption, compared to multi-amplifier biquads, e.g. integrator-connected biquads. Above these limits, the latter must be used.

1 Introduction

Single-amplifier biquadratic filters (SABs) need only one amplifier to generate a complex pair of poles. Compared to integrator-connected topologies, which need at least one amplifier per pole (e.g. Gm–C filters), they are more power-efficient and use less chip area. SABs are basically active-RC filters, but the low precision of passive components in CMOS makes it necessary to build fine-tunable filters, namely by using MOSFET resistors instead of poly-silicon resistors [1]. In this paper, we briefly discuss the theory behind such active-MOSFET-C Sallen-and-Key filters and show how a 25MHz biquad with a pole-Q of 3 and a spurious-free dynamic range of 45dB can be built in CMOS, which consumes only 2.4mW per pole and requires only 0.06mm^2 of chip area per pole.

The filter presented in this paper is a current-mode filter, for the following reason: the low-gain amplifier used to build a Sallen-and-Key filter can be implemented either as a high-gain amplifier with feedback or as a low-gain amplifier without feedback. With the latter, less power consumption and chip area is needed to implement a MOSFET-C filter of a certain pole frequency; the maximum achievable filter pole frequency is also higher for the latter. On the other hand, the missing feedback causes more harmonic distortion. Nevertheless, since we wanted to build filters with as high a pole frequency and as low a power consumption as possible, we chose to use an open-loop low-gain amplifier, which is easier to construct as a current rather than a voltage amplifier. Thus the filter presented in this paper operates in the current mode.

This paper consists of four parts. Section 2 gives a brief introduction into the theory of MOSFET-C SABs. The implementation of a balanced-signal CCCS based on class A current mirrors is briefly described in Section 3. In Section 4, the spurious-free dynamic range of the filter is discussed both theoretically and by measurements of a test chip. In the final Section we discuss in which ways our filter can be improved.

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2 Active-MOSFET-C single-amplifier biquads

The ideas underlying single-amplifier biquadratic filters (SABs) are old and well known, but since SABs are scarcely used on CMOS ICs, we will now briefly review their theory. After presenting the four main classes of SABs, we pick the most versatile class and discuss the effects of amplifier nonidealities, the expected variance of the pole Q, the implementation of such SABs as MOSFET-C filters, and the realisation of higher-order filters as cascades of second-order sections.

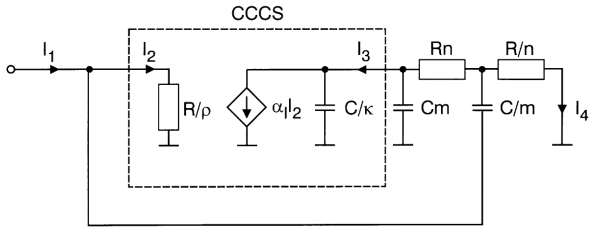

Fig. 1 *Class 4 current-mode lowpass filter*

2.1 SAB classification

Fig. 1 shows a current-mode active-RC lowpass filter. It consists of a current-controlled current source (CCCS) and a second-order RC network. Note that I_3 is drawn as flowing into the CCCS output, i.e. currents flowing into this output are defined as positive. For a general RC network, the transfer function of a single-feedback SAB can be expressed in terms of the transfer functions of the passive network alone,

$$t_{32} = \frac{I_2}{I_3} = \frac{n_{32}}{\hat{d}} \qquad t_{34} = \frac{I_4}{I_3} = \frac{n_{34}}{\hat{d}} \qquad (1)$$

and the amplifier gain α_I. Note that both t_{32} and t_{34} have

the same denominator, which is a quadratic term in s:

$$\hat{d} = a_2 s^2 + a_1 s + a_0 \qquad s_{1,2} = \frac{-a_1 \pm \sqrt{a_1^2 - 4a_0 a_2}}{2a_0} \tag{2}$$

where $s_{1,2}$ are the two real poles of both t_{32} and t_{34}. The transfer function then becomes

$$T(s) = -\alpha_I \frac{n_{34}}{\hat{d} + \alpha_I n_{32}} = -\alpha_I \frac{\omega_p^2}{s^2 + \frac{\omega_p}{q_p} s + \omega_p^2} \tag{3}$$

The poles of $T(s)$ become complex if α_I and n_{32} are chosen such that the argument of the square root in eqn. 2 becomes negative. There are four possible choices of n_{32}, corresponding to the four filter classes defined in [2, 3]: class 1 with $n_{32} = b_0$ (meaning that there is a lowpass filter in the feedback path); class 2, $n_{32} = b_2 s^2$ (highpass); class 3, $n_{32} = b_0 + b_2 s^2$ (band-reject) and class 4, $n_{32} = b_1 s$ (bandpass). It is obvious that classes 1–3 require a positive α_I, while class 4 requires a negative α_I. Note that, due to the definition of I_3's direction, the latter causes positive feedback. The filters in class 4 are conventionally called 'Sallen-and-Key filters' after the inventors of some of these filters [4].

Class 4 is the only class containing lowpass, highpass, band-reject and bandpass filters as well as allpass filters. It also has the advantage that its ω_p and q_p are orthogonal in the sense that ω_p can be tuned without affecting q_p. This becomes apparent in every concrete case, e.g. for a lowpass filter, when the passive components are expressed by R, C, m and n, as shown in Fig. 1. The location of the complex pole pair is then given by

$$\omega_p = \frac{1}{RC} \qquad q_p = \left(\frac{1}{mn} + mn + \frac{1}{n}\left(\frac{\alpha_I}{m} + m\right) \right)^{-1} \tag{4}$$

and ω_p can be tuned by adjusting the value of R, which will be explained later.

2.2 CCCS nonidealities

A non-zero input resistance R/ρ, a non-zero output capacitance C/κ and a non-zero phase lag of the amplifier gain α_I all shift the location of the poles, which can be accounted for by pre-distortion of the component values; for example, in the lowpass filter, C/κ is just connected in parallel to Cm. In this case, there are limits to how much pre-distortion can be made, since on the IC the parasitic capacitance C/κ is less linear than the poly–poly capacitance Cm. In addition to pole shifts, some of the nonidealities also cause parasitic zeros. In the case of the lowpass filter, the CCCS input resistance will cause a high-Q pair of complex zeros at a frequency of roughly $\rho\omega_p$ [5]. Although this makes the transfer function steeper close to the zeros, it also causes it to level out at a magnitude of α_I/ρ for higher frequencies and thus limits the filter's stopband attenuation.

2.3 Pole-Q variations

Since the sensitivity of q_p to variations of m, n and α_I is comparatively high (and proportional to q_p^2 in the latter case), it is important to use the degree of freedom available in choosing m, n and α_I to minimise the expected variance of q_p, $\bar{\sigma}_{q_p}^2$. The optimum gain of the CCCS can then be calculated from the variances of the passive and active component values. It is always below two, as demonstrated in [6]. However, since these variances are not easily determined for a given CMOS process, it is better to start off with a gain below two, check with a Monte Carlo simulation whether the resulting $\bar{\sigma}_{q_p}^2$ is acceptable, and redesign the circuit if $\bar{\sigma}_{q_p}^2$ is too high. Note that the optimum lowpass filter meets the following criteria [6]: $\alpha_I \le 2$, $m < 1$, $n > 1$ and $n < 1/m$ (i.e. the resistor spread is smaller than the capacitor spread). Note also that $\bar{\sigma}_{q_p}^2$ monotonically decreases for a constant α_I if m is reduced (i.e. the capacitor spread is increased).

2.4 Tunable SABs

To make active-RC filters tunable, they can be transformed into active-MOSFET-C filters by replacing the resistors with MOSFETs operating in the triode region. The resistances of these MOSFETs are then adjusted by their common gate voltage, V_C [1]. Using MOSFET resistors introduces strong harmonic distortion, but since the distortion is mainly of second order, it can be cancelled out almost completely by using a balanced design for the active-MOSFET-C filter, as in the SAB shown in Fig. 2. This idea has long and successfully been used to build integrator-connected MOSFET-C filters (c.f. [7, 8] or [9], Chap. 15.6). Since the term 'MOSFET-C filters' is conventionally used to denote integrator-connected filters only, [Note 1] we call our filters 'active-MOSFET-C SABs' to distinguish them from integrator-connected filters, and to relate them to their origin, the active-RC filters.

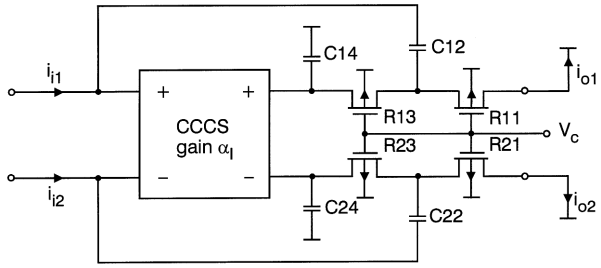

Fig. 2 *Balanced current-mode class 4 lowpass filter*

2.5 Biquad cascades

Finally, since the input resistance of active-MOSFET-C SABs is much lower than their output resistance, they can be cascaded to build higher-order current-mode filters. Finding the optimum sequence of the biquads in a cascade is by no means trivial. Most designers place the biquad with the highest f_p and q_p first, because its noise is then filtered by the remaining biquads, which follow either in descending or alternating order. A discussion of cascade sequences, pole–zero pairing and gain distributions can be found in [11]. Note that we have taken the possibility of building biquad cascades into account by loading all filter outputs with 750Ω for measurements and simulations, which is slightly more than the CCCS's input resistance (c.f. Section 3.2).

3 Implementation of a balanced CCCS

To implement the filter shown in Fig. 2, it is necessary to build a balanced CCCS which is as symmetrical as possible, since any asymmetry will cause second-order harmonic distortion in the filter output. Furthermore, the input resistance should be low enough to guarantee a sufficient stopband attenuation, as described in Section 2.2. In this Section, we first present one possible implementation of a CCCS, then we briefly discuss local feedback and our reasons for not using it, and finally we present some measurement results.

Note 1: We know of only one implementation of a MOSFET-C SAB, which was done using a BiCMOS process [10].

3.1 Differential-input balanced-output CCCS

The CCCS used in our filters has already been described in [12], and thus only a brief description is included here. To ensure the best possible symmetry, our CCCS consists of two identical paths, as shown in Fig. 3. Ideally, it is described by

$$i_{o1} = \alpha_I(i_{i1} - i_{i2}) \qquad i_{o2} = -\alpha_I(i_{i1} - i_{i2}) \qquad (5)$$

This means that a current difference must be formed, amplified, and mirrored to two outputs with different signs.

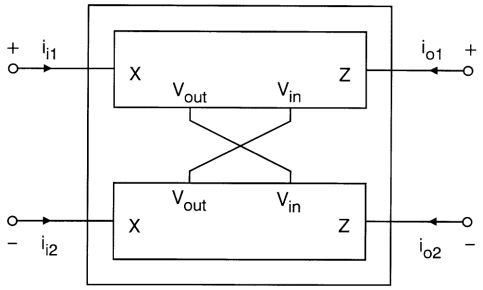

Fig. 3 *Block diagram of CCCS*

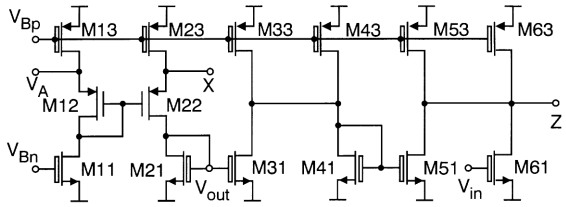

Fig. 4 *One half of CCCS*

This is achieved by the half-circuit shown in Fig. 4, which consists of one voltage buffer and several class A current mirrors. The purpose of the voltage buffer is to provide a low-impedance input at node X at a voltage of V_A, the analogue ground. Any current flowing into X is mirrored twice and flows out of Z; it is also mirrored once and flows into the Z-terminal of the other half-circuit. Thus the signal subtraction is actually done at the CCCS's outputs. Note that the DC gain of this CCCS is $\alpha_I = -2$ if unity-gain current mirrors are used. A different gain can be achieved by resizing M51, M53, M61 and M63. As explained in Section 2.3, $|\alpha_I|$ must be below two at the pole frequency. In our case, this meant using a DC gain of –2.6 to achieve $\alpha_I = -1.9$ at $\omega_p = 2\pi \times 24$ MHz. The reason for allowing so much gain roll-off towards ω_p is power consumption: to make the CCCS as power efficient as possible, it is designed such that the phase lag at the filter's pole frequency is as large as acceptable [5], 25 degrees in our case.

This CCCS was implemented in a 0.6μm double-poly CMOS process (c.f. Table 1 for process parameters and Table 2 for transistor dimensions). V_A was set to the mid-rail voltage, and all transistors drawn with boxed gates were implemented as two-transistor cascodes whose cascode transistors were biased by the mid-rail voltage as well, with the exception of M11's cascode transistor, which needs a lower bias voltage to make room for the gate-source voltage of M12 (the voltage V_{bc} in Fig. 5).

Table 1: Typical threshold voltages, transconductance parameters, body factors, characteristic potentials and noise correction factors (c.f. Section 4.2) of the 0.6μm CMOS process used for building the test chip

	nMOS	pMOS	Unit
V_{T0}	0.85	–0.92	V
$\mu \cdot C_{ox}$	120	40	μA/V²
γ	0.8	0.5	√V
ϕ_0	0.94	0.91	V
$\alpha_{n,p}$	2.35	1.30	

Table 2: Transistor and double-poly capacitor dimensions

	Capacitor dimensions, μm	Capacitance, pF
C[1–2]2	13.6 × 13.6 × 10	1.0
C[1–2]4	13.6 × 13.6	0.1
	Main transistors, μm	Cascode transistors, μm
M[1–4]1	45 × 3	80 × 0.6
M[5–6]1	57.3 × 3	104 × 0.6
M81	37.3 × 3	—
M91	45 × 3	80 × 0.6
M[1–2]2	120 × 0.6 × 2	—
M[1–4]3	120 × 3	200 × 0.6
M[5–6]3	200 × 3	260 × 0.6
M[7–9]3	120 × 3	200 × 0.6
R[1–2]1	22 × 2.4 × 2	—
R[1–2]2	22 × 1.9 × 2	—

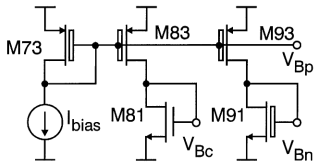

Fig. 5 *Bias circuit*

3.2 Making the CCCS more ideal

The output capacitance of the CCCS is 0.38pF, while its input resistance is $R_{in} \simeq 1/g_{m22} = 550\Omega$. There are two ways of decreasing the CCCS's input impedance. One is to make M12 and M22 wider, but this increases the phase lag of the CCCS and must be compensated by making the CCCS faster, i.e. by increasing the bias current and therefore the power consumption. Doing this also increases the CCCS's noise, as explained in Section 4.2.

A different idea is to use local feedback in the input voltage buffer. The problem with this approach is that the current input then behaves inductively at the filter pole frequency. The effective reduction of the input impedance is proportional to the feedback loop gain. However, since we want to reduce R_{in} because of the parasitic zeros it causes, the feedback loop gain at the zero frequency is relevant. In our filter, these zeros are around 100MHz, meaning that the unity-gain frequency of such a feedback loop must be several hundred MHz to increase the stopband attenuation and with it the maximum possible pole frequency by only a small factor. In addition, the feedback loop needs to have a phase margin of at least 55 degrees to avoid ringing. While all this is feasible, it costs substantial amounts of power and chip area (c.f. [13]). Thus we decided not to use local feedback for our feasibility study.

3.3 Measurements

Fig. 6 shows the transfer functions of the filters on 14 chips [Note 2]. The measured mean values are $f_p = 24.2$MHz and $q_p = 3.1$, both very close to the values simulated with typi-

Note 2: One of 15 produced chips had a short between V_{dd} and V_{ss}.

cal transistor parameters, f_p = 22.3MHz and q_p = 3.0. The ideal transfer function is drawn with a dashed line to make the influence of the parasitic zeros visible. The standard deviations of ω_p and q_p are only 1.5% and 3%, respectively, for these 14 filters coming from the same process run. The absolute value of f_p was very close to the simulated value due to the fact that the process run in which the chips were produced happened to have typical parameters. It was also found that the variance of q_p is mainly due to the variance of the component spreads, and the gain is more than stable enough. Thus the current mirror transistors can be made shorter, which makes it possible to decrease both the CCCS's phase lag and chip area and to build filters with a higher pole frequency.

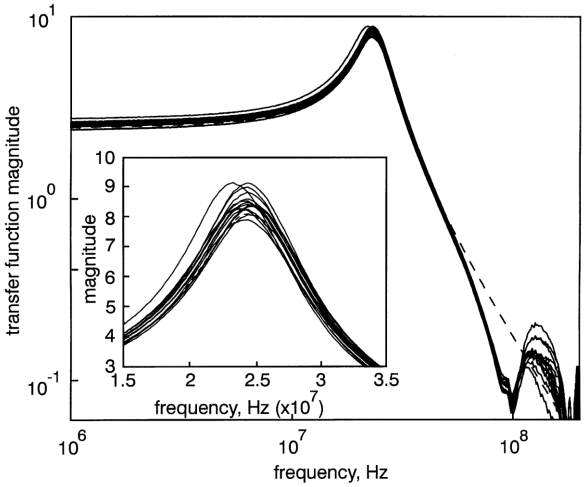

Fig. 6 *Measured filter transfer function on all 14 chips*
– – – ideal transfer function
Inset: Close-up picture of peak

4 Spurious-free dynamic range

The main noise contribution comes from the CCCS, while harmonic distortion is caused both by the CCCS's output stage and the MOSFET-C network. The maximum spurious-free dynamic range is achieved for the signal magnitude for which harmonic distortion and noise are equally strong. We now discuss both harmonic distortion and noise, and then derive the SFDR of the filter from measurements. It will become clear why our choice of V_A in the preceding Section was not good at all, and how much SFDR can be won by correcting the choice.

4.1 Harmonic distortion

In [8], the harmonic distortion of a MOSFET-C integrator was derived as a function of the signal magnitude. Repeating a similar calculation for a MOSFET-C SAB leads to formulae of prohibitive complexity. Fortunately, if the filter to be designed is a video-frequency filter with a spurious-free dynamic range of 40–55dB, then such a detailed analysis is not really necessary. The reason is that harmonic distortion of that order of magnitude only occurs when some signal clipping sets in.

There are two effects in a MOSFET-C biquad that lead to signal clipping. First, if any terminal voltage of a MOSFET resistor goes too close to the gate, then the MOSFET saturates. Secondly, if the output terminal voltage of the CCCS goes too close to either rail, then the respective cascode transistor leaves the saturation region, and the CCCS output resistance drops. Since the clipping is similarly hard in both directions, it makes sense to choose the analogue signal ground voltage V_A in the middle between the pinch-off voltage of the MOSFET resistors and the voltage where all cascode transistors are just saturated. According to [14], the pinch-off voltage becomes

$$V_p = \frac{V_C - V_{T0}}{m_0} \quad \text{with} \quad m_0 = 1 + \frac{\gamma}{2\sqrt{V_A + \phi_0}} \tag{6}$$

where V_C is the gate control voltage of the MOSFET resistors, and m_0 is a body effect parameter (c.f. Table 1 for the other parameters). Note that all voltages are related to the MOSFET resistor's bulk, i.e. to V_{dd} for a *p*MOS and to V_{ss} for an *n*MOS resistor.

In our design, we chose V_A = 1.65V, i.e. the middle between the rails, and V_C = 3.3V. Therefore V_p = 2.07V for *p*MOS resistors and V_p = 1.90V for *n*MOS resistors. Thus *p*MOS resistors are preferred, because they offer a higher voltage swing and therefore a better SFDR. The resistance of a MOSFET resistor is [14]

$$R_{pMOS} \simeq (K\,(V_G - V_{T0} - m_0 V_A))^{-1} \tag{7}$$

At low frequencies, the capacitors in Fig. 2 are not effective, and R11 and R12 act as one single *p*MOS resistor of size 44 × 4.3μm. Thus R_{pMOS} = 5.1kΩ in our example. The maximum possible voltage swing before pinch-off occurs is

$$V_{max} = V_p - V_A \tag{8}$$

making V_{max} = 0.42V. Finally, the maximum signal current which can flow through the MOSFET resistors is the saturation current of the *p*MOS resistor,

$$I_{max} = I_{sat} = K\,(V_G - V_{T0} - m_0 V_A)^2 \tag{9}$$

and therefore I_{max} = 42μA. This is the maximum output current of the filter; with reference to the input, the maximum current is only 16μA.

It can easily be seen that the choice V_A = 1.65V is not good, since the voltage can only swing by V_{max} = 0.42V towards the negative rail but by a full threshold voltage V_{T0} = 0.85V towards the positive rail, with M63's cascode still being saturated. As discussed above, V_A should be set between V_p and V_{min},

$$V_A = \frac{V_p + V_{min}}{2} \tag{10}$$

If the cascodes are biased by the mid-rail voltage, $V_{dd}/2$, then $V_{min} = V_{dd}/2 - V_{T0}$ = 0.73V. Inserting eqn. 10 into eqn. 6 results in

$$V_A - \frac{V_{min}}{2} = \frac{(V_G + V_{T0})\sqrt{V_A + \phi_0}}{\gamma + 2\sqrt{V_A + \phi_0}} \tag{11}$$

whose symbolic solution does not provide much insight. Solving it numerically for the process parameters in Table 1 results in V_A = 1.4V, which is 0.25V closer to V_{dd} than the local analogue ground we chose on our chip. It can be seen from eqn. 7 that moving the analogue ground to V_A = 1.4V reduces the sheet resistance by a factor of 1.57. Thus, for maintaining the same resistance, the width of the MOSFET resistors must be increased from 44μm to 69μm. Then the new saturation current can be calculated as before using eqn. 9, resulting in I_{max} = 158μA. Therefore, simply moving the analogue ground by 0.25V towards the positive rail increases the maximum allowable current by a factor of 3.76, or 11.5dB.

Note that choosing the optimum V_A for *p*MOS resistors increases the voltage margin available for operating M11. On the other hand, moving the analogue signal ground towards the negative rail, as would be necessary with *n*MOS resistors, would make M11 almost inoperable. *n*MOS resistors could therefore only be used if *n*MOS

instead of *p*MOS transistors were used in the voltage buffer. This is, however, not advisable in an *n*-well process such as ours, and even in a *p*-well process it would mean that the actual current mirroring would have to be performed by *p*MOS transistors, decreasing the speed of the CCCS.

4.2 CCCS and filter noise

The white noise of the CCCS can be calculated by referring the noise current contributions of all transistors to the output of the CCCS. Since there are defined relationships between most of the transistors in the CCCS, it is possible to express all noise contributions in terms of the white noise spectral density of M33's drain current, inserting eqn. 10 into eqn. 6 results in

$$i_{\mathrm{M33}}^2 = 4\hat{k}T \cdot \frac{2}{3}\alpha_{\mathrm{p}} g_{\mathrm{m33}} \tag{12}$$

where α_{p} is a noise correction factor (see Table 1) [14]. The noise contributions of all transistors at the CCCS output can then be added, but note that the noise of a single transistor travelling along paths with different signs will not cancel at the output because the different paths have different time delays. Keeping the width of the bias transistor and the ratio of the aspect ratios of M22 and the aspect ratio of M33 as free parameters, we obtain

$$i_{\mathrm{CCCS}}^2 = 2i_{\mathrm{M33}}^2 \left(\alpha_{\mathrm{I}}^2 \left[\frac{\alpha_{\mathrm{n}}}{\alpha_{\mathrm{p}}} \sqrt{\frac{L_{22}}{W_{22}} \frac{W_{33}}{L_{33}}} + \frac{3}{2}\left(1 + \frac{\alpha_{\mathrm{n}}}{\alpha_{\mathrm{p}}} + \sqrt{\frac{W_{73}}{W_{33}}}\right) \right] + \frac{\alpha_1}{2}\left(1 + \frac{\alpha_{\mathrm{n}}}{\alpha_{\mathrm{p}}}\right) + 2\sqrt{\frac{W_{73}}{W_{33}}} \right) \tag{13}$$

In our example, this is approximately $160 i_{\mathrm{M33}}^2$. Of this noise, 70% are produced by current mirrors and current sources, 20% by the input transistors M12 and M22, and 10% by the bias transistor M73. This results in i_{CCCS} = 36pA/√Hz.

The white noise of the CCCS is then shaped by the SAB and can be calculated approximately using the noise bandwidth of the filter, f_{x} ([9], Chap. 4):

$$i_{\mathrm{Filter(RMS)}}^2 \simeq i_{\mathrm{CCCS}}^2 \cdot f_{\mathrm{x}} \tag{14}$$

where f_{x} can be derived from the filter's ideal transfer function,

$$f_{\mathrm{x}} = \int_0^\infty \left| \frac{1}{-\frac{f^2}{f_{\mathrm{p}}^2} + j\frac{f}{f_{\mathrm{p}} q_{\mathrm{p}}} + 1} \right| \mathrm{d}f = \frac{\pi}{2} q_{\mathrm{p}} f_{\mathrm{p}} \tag{15}$$

Note that the same f_{x} results for the second-order bandpass filter.

4.3 Measured SFDR

Fig. 7 presents measurements of the output-referred noise of both the filter and a separate CCCS on the chip. Note how close the calculated i_{CCCS} = 36pA/√Hz is to the measured 45pA/√Hz. The curve denoted by 'i_{shaped}' is the CCCS's noise shaped by the filter transfer function, while 'i_{Filter}' is the measured filter noise spectral density. The two curves agree closely, which means that the noise contribution by the passive network is negligible. Inserting the measured CCCS white noise into eqn. 14 results in an output noise current of 480nA$_{\mathrm{RMS}}$ for f_{p} = 24MHz and q_{p} = 3.

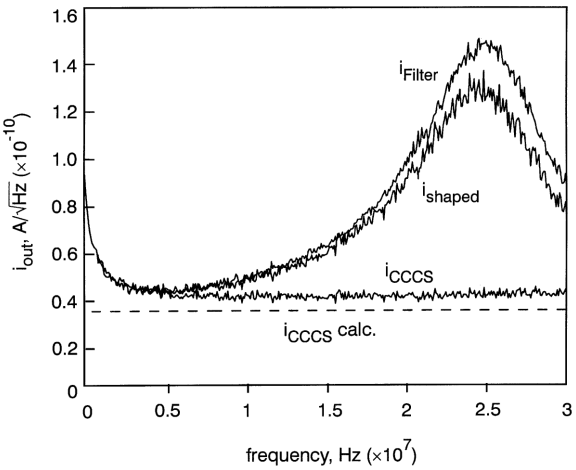

Fig. 7 *Noise: output-referred power spectral densities*

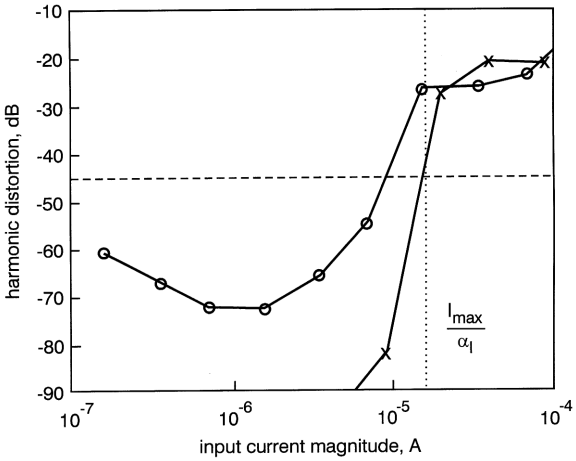

Fig. 8 *Low-frequency (50kHz) harmonic distortion of filter*
—○— measured
—×— simulated

Fig. 8 shows the simulated and measured total harmonic distortion for a low-frequency signal in function of the input signal current. The simulation, made without taking mismatch into account, predicts that –45dB of harmonic distortion is reached precisely for the maximum output current I_{max} calculated in Section 4.1, which is 16μA if referred to the input. The measured THD reaches –45dB already at 9μA. Simulation and measurement disagree by 5dB of input signal magnitude. Conventionally, the THD of a low-pass filter is measured at one-fifth of the pole frequency, or at 5MHz in our case. These measurements are shown in Fig. 9. The maximum allowable input current is 7.3μA according to simulation and only 4μA according to the measurements. Again, the factor between the simulated and measured value is 5dB. Therefore it seems reasonable to assume that this factor is due to mismatch between the two signal paths. Note that the harmonic distortion is much higher for high frequencies, because the nonlinear output capacitance of the CCCS, C_{out} = 0.38pF, is large compared to the linear poly-poly capacitance of 0.1pF connected to the same node. Since this configuration is almost the worst case, it can be assumed that the factor of 12dB between the I_{max} calculated according to Section 4.1 and the value which must be expected in measurements can be used as a rule of thumb for designing active-MOSFET-C SABs.

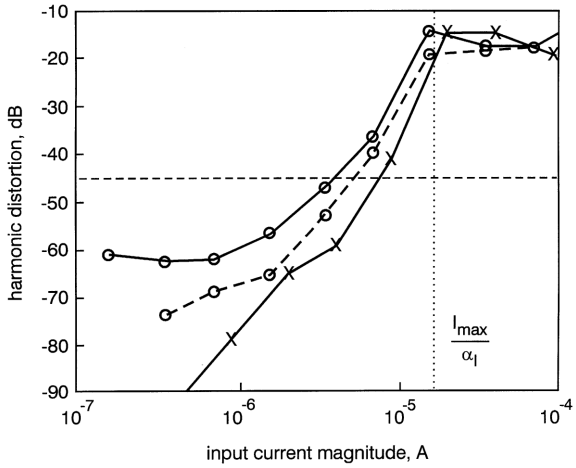

Fig. 9 *Harmonic distortion at 5MHz*
—○— measured
– –○– – odd-order
—×— simulated

According to the 5MHz measurement, the output current of the filter may reach 10.4μA, or 7350nA$_{RMS}$ at the output. Therefore the signal-to-noise ratio is only 24dB, which is 21dB below the mark. However, if V_A is moved towards V_{dd}, as suggested in Section 4.1, then 12dB is gained, and we are now only 9dB (a factor of 2.8) below the mark. Another 6.5dB can be won by moving V_A 300mV further towards the positive rail, but then it is necessary to move the bias voltage of the *p*MOS cascode transistors up as well, and therefore to widen all transistors in the constant current sources. On the other hand, the *n*MOS current mirrors can then be made smaller. We are confident that the remaining 2.5dB (a factor of 1.33) can be gained by optimising all transistor sizes (especially the size of M73) with respect to noise.

Table 3: Measured properties of lowpass biquad

Pole frequency	24MHz
Pole Q	3
Supply voltage	3.3V
Min. feature size	0.6μm
Power consumption	4.8mW
Chip area	0.12mm^2
SFDR	24 (→ 45)dB
Min. PSRR (V_{dd})	51dB[a]
(V_{ss})	49dB

[a]The worst-case PSRR was obtained through Monte Carlo simulations. Since the PSRR is lowest at the filter pole frequency, a 24MHz, 0.1V signal was fed into the power supply. This caused a distortion current which was multiplied by 500Ω, the input resistance of the biquad, in order to calculate a power-supply rejection ratio

5 Discussion and conclusions

The discussion in the preceding Section is based on our experience with various test circuits and on simulations of the extracted layout using typical, worst-case and specially tailored Monte Carlo transistor models provided by the foundry. Some measured values are presented in Table 3. We have shown that the comparatively low SFDR of the test filter can be increased to around 45dB. Using the techniques and the CCCS implementation presented in this paper, we measured a 25MHz filter with a pole-Q of three, corresponding to a noise bandwidth of 120MHz. Note that, within this limit, a 16MHz, seventh-order Bessel filter, e.g. for video applications, can readily be built, whose highest-Q biquad then typically consumes around 5mW (2.5mW per pole).

Comparisons with recently published integrator-connected filters (Gm–C [15–18] and MOSFET-C [19]) show that our active-MOSFET-C SABs generally use less power and a smaller chip area than Gm–C filters. MOSFET-C SABs are, however, limited in performance, mainly due to the MOSFET resistors which limit the available voltage swing at the nodes of the MOSFET-C network, and the current mirrors which limit the achievable SNR. With the 0.6μm process we used, video-frequency biquadratic filters with (i) a noise bandwidth below 120MHz, (ii) a spurious-free dynamic range no higher than 55dB (45dB at a noise bandwidth of 120MHz, more at lower frequencies), (iii) a pole-Q lower than about 8, and (iv) a V_{dd} not far below four transistor threshold voltages (3.3V for our process having threshold voltages of 0.85V) can be built. If any of the filter specifications lies outside these boundaries, then a different technique must be used to build the filter.

Alternatively, the physical design of the filter can be modified in several nontrivial ways to reach higher frequencies. Possibilities are:

(i) Use local feedback in the input stage to reduce the CCCS's input resistance (c.f. Section 3.2). This allows the MOSFET resistances to be made smaller and therefore to increase the maximum allowable signal current without adding much noise. It does, however, considerably increase the power consumption and the chip area, and can introduce ringing and possibly slewing problems.

(ii) Use wide-swing *p*MOS current sources ([9], Chap. 6.1) or regulated cascode techniques [13, 20] at the CCCS outputs. Both allow the voltage swing towards V_{dd} to be increased without increasing (or even while decreasing) the output capacitance and without increasing noise. However, the phase lag of the CCCS will then increase as well.

(iii) If the process used for building the filter permits, a control voltage V_C outside the rails can be used, generated by a charge pump [21]. This makes it possible to increase the maximum allowable signal current considerably. However, since a charge pump can never generate a voltage below V_{ss}, *n*MOS instead of *p*MOS resistors must be used in this case, and a different CMOS input stage must be used. Clock feed-through may also be a problem, but low-ripple charge pumps for similar applications have been built successfully [22].

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