On Sequential Analog-To-Digital Conversion with Low-Precision Components

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***Abstract*— It was shown in prior work that, with proper digital calibration, ADCs with high static resolution can in principle be built without precise analog components. The paper offers some afterthoughts on this topic and connects it with beta expansions. It is suggested that, with proper calibration (but not without), ADC architectures based on the beta expansion can indeed achieve an effective resolution of m bits with analog circuit complexity linear in m and without precise analog components.**

I. Introduction

The static accuracy of certain analog-to-digital converters (ADCs) with low-precision components and digital correction was studied in [1], [2]. In this paper, we continue the discussion in [2] and connect it with the work by Daubechies et al. on ADCs based on beta expansions [3]–[5]. As in [1], [2], we will consider only the static accuracy of ADCs; both noise and dynamic issues (including the thorny practical problem of accurate sampling) will be ignored in this paper.

Our interest will be in sequential ADC schemes that do not require precise analog circuits (but do need digital calibration). The necessary background and the motivation will be given in Section II. In particular, it will be pointed out that such an ADC (with attractive analog complexity) may be obtained by using the digital-to-analog converter (DAC) of [2] in a successive-approximation ADC scheme.

Nevertheless, a more direct "robustification" of the ideal sequential ADC (cf. Section II) is desirable. A promising step in this direction was made by Daubechies et al. in [3]–[5]. By using beta expansions, exact comparators are no longer needed. However, exponentially precise analog computations are still required. We will review this approach in Section IV.

Generalizations of this approach will be considered in Section V. These generalizations do not require precise analog computations, but some sort of digital calibration. For a simplified version of such a scheme, the effective resolution is assessed by simulations. We will conclude that such schemes may be attractive and deserve further study.

II. Background and Motivation

Let x be the real number in the analog domain that we wish to convert into the digital domain and let $\hat{x} \in \mathbb{R}$ be the resulting digital approximation of x. Without loss of generality, we will assume $0 \le x < 1$. As in [2], we will measure the accuracy of an ADC in terms of its effective resolution (in bits), which is defined as

$$\text{Res}_{\text{eff}} = -\log_2 \sqrt{12 \cdot \text{MSE}} \tag{1}$$

where MSE denotes the mean squared error

$$\text{MSE} = \int_0^1 (\hat{x}(x) - x)^2 dx. \tag{2}$$

Let us begin by recalling two standard ADC schemes and the "random" flash ADC of [2].

Ideal Sequential ADC. Let $x_1 \triangleq x$ and let $x_2, x_3, \ldots, x_N \in \mathbb{R}$ and $b_1, b_2, \ldots, b_N \in \{0, 1\}$ be defined by the recursion

$$x_{k+1} = 2x_k - b_k \tag{3}$$

with

$$b_k = \begin{cases} 0, & \text{if } x_k < 1/2 \\ 1, & \text{if } x_k \ge 1/2 \end{cases} \tag{4}$$

Then

$$\hat{x} = \sum_{k=1}^{N} b_k 2^{-k} \tag{5}$$

□

This ADC scheme provides the bits $b_1, \ldots, b_N$ of $\hat{x}$ in the standard digital representation in N steps and its effective resolution (1) is N bits. The problem with this scheme is that both (3) and (4) need to be performed by analog circuits and with sufficient precision. The cost of such circuits in terms of chip area (and therefore also in terms of power consumption) grows exponentially with N and is unaffordable unless N is very small.

Ideal Flash ADC. The analog input x is fed in parallel to K comparator circuits. Each comparator has its own threshold $\theta_k = k\Delta$ with $\Delta = 1/(K+1)$ and it computes as digital output the sign of $x - \theta_k$. If $\theta_k \le x < \theta_{k+1}$, we have

$$\hat{x} = k\Delta + \Delta/2. \tag{6}$$

□

This ADC scheme provides an effective resolution of $\log_2(K+1)$ bits. The required accuracy (and thus the chip area and the power consumption) of each comparator is linear in K, i.e., exponential in the effective resolution.

However, it was shown in [2] that the precision of the comparators can be reduced almost arbitrarily if digital calibration is used.

"Random" Flash ADC with Digital Calibration. As with the ideal flash ADC, we have K comparator circuits, but now with arbitrary thresholds θ_k, $k = 1, \ldots, K$. For the sake of clarity, we will define the dummy thresholds $\theta_0 = 0$ and $\theta_{K+1} = 1$ and assume $\theta_k < \theta_{k+1}$ (after reordering, if necessary). If $\theta_k \le x < \theta_{k+1}$, we have

$$\hat{x} = (\theta_k + \theta_{k+1})/2. \tag{7}$$

□

The MSE (2) of such an ADC is

$$\text{MSE} = \frac{1}{12} \sum_{k=0}^{K} (\theta_{k+1} - \theta_k)^3. \tag{8}$$

The following observations were made in [2]:

1) If the thresholds θ_k are distributed uniformly between 0 and 1, then the expected effective resolution (in bits) is

$$\text{Res}_{\text{eff}} = \log_2 K - \log_2 \sqrt{6} \tag{9}$$

$$\approx \log_2 K - 1.29 \text{ bits} \tag{10}$$

   in the limit of $K \to \infty$.
2) Even slight deviations (as well as large deviations) from the ideal flash ADC (where $\theta_k = k\Delta$) tend to yield an effective resolution close to the asymptotic value (9).

It follows that such an ADC does not need precise comparators and may therefore be attractive. However, with cheap comparators, the thresholds θ_k will vary from chip to chip and need to be measured somehow. Moreover, the number of comparators still grows exponentially with the effective resolution.

Having thus set the stage, it is natural to ask whether some sort of calibrated sequential ADC scheme exists that retains the compactness and elegance of the ideal sequential ADC but does not need precise analog computations.

III. Successive-Approximation ADC with DAC from [2]

A sequential ADC with many of the desired properties may actually be obtained by using the DAC of [2] in a successive-approximation ADC [6]. Indeed, the main result of [2] is the observation that current steering DACs with N "small" (i.e., near-unit size) and imprecise current sources can achieve an effective resolution of about $N - 2$ bits. The same effective resolution is achieved when such a DAC is used in a successive-approximation ADC, which requires no additional analog circuits except for a single comparator (which may even have an offset).

However, we will continue on a different path.

IV. On Beta Expansion ADCs

A beta expansion ADC [3]–[5] is a generalization of the ideal sequential ADC as follows.

Beta Expansion ADC. Let β be a real number such that $1 < \beta \le 2$. Let $x_1 \triangleq x$ and let $x_2, x_3, \ldots, x_N \in \mathbb{R}$ and $b_1, b_2, \ldots, b_N \in \{0, 1\}$ satisfy the recursion

$$x_{k+1} = \beta x_k - b_k \tag{11}$$

where

$$b_k = \begin{cases} 0, & \text{if } \beta x_k < 1 \\ 0 \text{ or } 1, & \text{if } 1 \le \beta x_k < \frac{1}{\beta - 1} \\ 1, & \text{if } \beta x_k \ge \frac{1}{\beta - 1} \end{cases} \tag{12}$$

Then

$$\hat{x} = \sum_{k=1}^{N} b_k \beta^{-k} \tag{13}$$

□

Note that (13) converges to x for $N \to \infty$.

In the middle case of (12), b_k may be chosen freely. If the difference

$$\frac{1}{\beta - 1} - 1 = \frac{2 - \beta}{\beta - 1} \tag{14}$$

is sufficiently large, the comparison in (12) may thus be carried out by a low-precision comparator. However, the analog computation of (11) still requires a precision (and the corresponding chip area and power consumption) that is exponential in the effective resolution.

It was shown in [5] that the parameter β need not be known in advance, but can be estimated accurately from the digital output. While this is good news, it does not remove the necessity of exponential precision in the computation of (11).

V. On Low-Precision Approximations of Beta Expansion ADC

Implementations of the computation (11) by low-precision (i.e., small) analog circuits will result in a modified recursion

$$x_{k+1} = f_k(x_k, b_k) \tag{15}$$

where $f_k(x_k, b_k)$ are unknown functions (indexed by k) that somehow approximate (11). While (13) no longer works in this case, such circuits may nonetheless be useful. In particular, they may be used with the correction (7), where the thresholds θ_k are those values of x where at least one bit b_k flips. The effective resolution is then given by (8).

In order to get some idea of the potential performance of such schemes, we consider generalizations of (11) with

$$x_{k+1} = \beta_k x_k - b_k(1 + \epsilon_k) \tag{16}$$

and with

$$b_k = \begin{cases} 0, & \text{if } \beta_k x_k < s_k \\ 1, & \text{if } \beta_k x_k \ge s_k. \end{cases} \tag{17}$$

Note that (16) and (17) are meant to be a toy model—not a realistic model—of a real analog circuit. We then consider ensembles of such ADCs where β_k, ϵ_k, and s_k are random variables so as to model component mismatch between nominally identical circuits. Specifically,

- β_k is a normal random variable with mean β and standard deviation σ_β.
- ϵ_k is a normal random variable with mean 0 and standard deviation σ_ϵ.
- s_k is a normal random variable with mean $\frac{\beta}{2(\beta-1)}$ (which is the middle point between 1 and $1/(\beta-1)$) and variance σ_s.

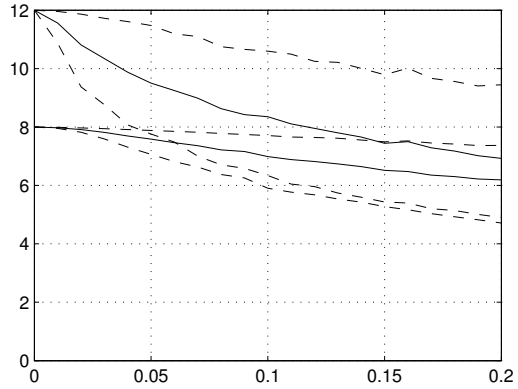

Fig. 1. Effective resolution vs. standard deviation σ (= $\sigma_\beta = 2\sigma_\epsilon = 2\sigma_s$) for $\beta = 2$ and $N = 12$ sections (top) as well as $N = 8$ sections (bottom).

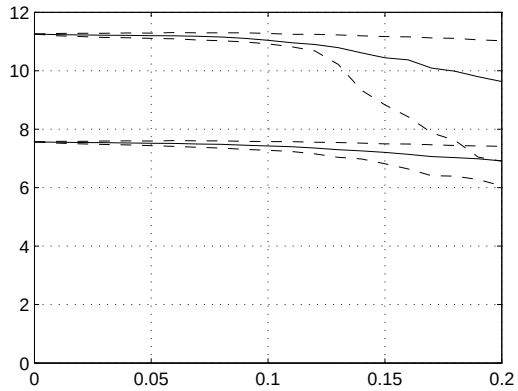

Fig. 2. Effective resolution vs. standard deviation σ (= $\sigma_\beta = 2\sigma_\epsilon = 2\sigma_s$) for $\beta = 1.8$ and $N = 12$ sections (top) as well as $N = 8$ sections (bottom).

Some simulation results for such ADCs are given in Figures 1–3. All these plots show the effective resolution (according to (1) and (8)) vs. the standard deviation $\sigma = \sigma_\beta$ and with $\sigma_\epsilon = \sigma_s = \sigma/2$. In all three figures, results are shown both for $N = 12$ sections (top) and for $N = 8$ sections (bottom). In each figure, the solid line represents the average effective resolution and the dashed lines represent the top tenth percentile and the bottom tenth percentile of the simulated ensemble.

In Fig. 1, we have $\beta = 2$; this ensemble is not very robust, especially for $N = 12$. In Fig. 2, we have $\beta = 1.8$, which results in much more robust performance. In Fig. 3, we have $\beta = 1.5$, which extends the range of robust performance at the expense of a reduced resolution for small σ.

These simulations confirm the suggestion that, with proper digital calibration, ADCs based on the beta expansion can indeed do without precise analog computation.

Note that we did not propose a practical calibration scheme, but the simulation results give motivation to study such schemes.

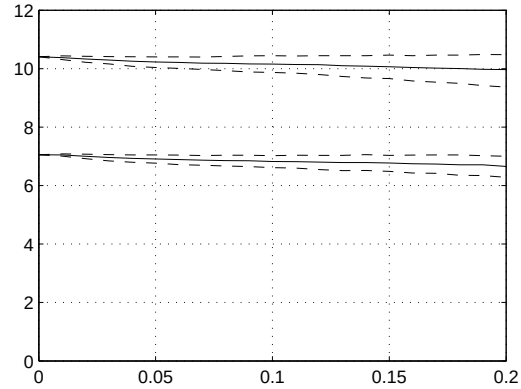

Fig. 3. Effective resolution vs. standard deviation σ (= $\sigma_\beta = 2\sigma_\epsilon = 2\sigma_s$) for $\beta = 1.5$ and $N = 12$ sections (top) as well as $N = 8$ sections (bottom).

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