On the Static Accuracy of Digitally Corrected Analog-to-Digital and Digital-to-Analog Converters

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***Abstract*— Some basic observations are made about the static accuracy of ADCs and DACs with full digital correction. First, the accuracy of flash ADCs is considered. It is pointed out that the loss in effective resolution due to component mismatch is only about 1 bit, independently of the mismatch level (unless the mismatch is very small). Second, the accuracy of current steering DACs is considered. It is noted that current-source mismatch can hugely *improve* the effective resolution of DACs, and it is shown that an effective resolution of m bits can be achieved with as few as $m + 2$ "small" current sources.**

I. Introduction

Analog-to-digital converters (ADCs) often consume considerable amounts of power and silicon area. In current ADCs, a substantial fraction of these resources is spent to fight component mismatch, i.e., production time randomness, rather than noise, i.e., run time randomness. In fact, some popular digital correction methods ("dynamic element matching") combat mismatch by converting it into noise [1].

The attractivity of (static and dynamic) digital correction methods grows as the relative cost of digital circuitry continues to shrink.

Similar observations apply to digital-to-analog converters (DACs). In fact, ADCs are often built with an internal DAC, and the main limitation of such designs tend to come from the latter.

In this paper, we point out some basic observations on the influence of mismatch on the static accuracy of ADCs and DACs with full static digital correction.

First, we consider component mismatch in flash ADCs. We point out that, with proper digital correction, the loss in effective resolution due to mismatch is roughly 1 bit *independently of the actual mismatch level* (unless the mismatch is very small). In consequence, there is no point in spending resources to keep the mismatch small.

Second, we consider component mismatch in current steering DACs [2]. (Similar conclusions will apply also to other types of DACs). We point out that, with proper digital correction, mismatch can hugely *improve* the resolution over that of a comparable conventional "ideal" DAC. In fact, we demonstrate that an effective resolution of about m bits can be achieved by as few as $m + 2$ imprecise nearly-unit current sources.

II. Flash ADCs with Low-Precision Comparators

A flash ADC applies the analog input $x \in \mathbb{R}$ in parallel to K comparator circuits. Each comparator has its own threshold θ_k, $k = 1, \ldots, K$, and computes the sign of $x - \theta_k$. In order to simplify the following discussion, we will assume $0 \le x < 1$ and we define the two dummy thresholds $\theta_0 = 0$ and $\theta_{K+1} = 1$.

An ideal m-bit flash ADC has $K = 2^m - 1$ comparators with thresholds $\theta_k = k\Delta$, $k = 1, \ldots, K$, with $\Delta = 2^{-m}$. However, in this paper, we allow arbitrary thresholds.

Let $k_{\mathrm{L}}(x)$ be the index k of the largest threshold θ_k such that $\theta_k \le x$ and let $k_{\mathrm{U}}(x)$ be the index k of the smallest threshold θ_k such that $x < \theta_k$. Note that the joint output of all K comparators may be summarized by either k_{L} or k_{U}. The standard way of interpreting this output is as the real number

$$\hat{x}_{\text{standard}} = k_{\mathrm{L}}\Delta + \Delta/2, \tag{1}$$

which we will call the uncorrected output. An obvious alternative interpretation is

$$\hat{x}_{\text{corr}} = \left(\theta_{k_{\mathrm{L}}} + \theta_{k_{\mathrm{U}}}\right)/2, \tag{2}$$

which we will call the corrected output. For an ideal ADC, these two interpretations coincide.

Our main point is this: for an ADC with corrected output (2), the loss in accuracy due to non-ideal thresholds θ_k does not exceed about 1 bit (with very high probability).

We demonstrate this property by considering an ensemble of ADCs with random thresholds $\theta_k = k\Delta + E_k$, $k = 1, \ldots, K$, where $E_1, \ldots E_K$ are independent zero-mean Gaussian random variables with variance σ^2. We will measure the quantization distortion by the mean squared error (MSE) defined as

$$\text{MSE} = \int_0^1 \left(\hat{x}(x) - x\right)^2 dx, \tag{3}$$

and we define the effective resolution (in bits) as $-\log_2 \sqrt{12\,\text{MSE}}$.

Fig. 1 shows the average effective resolution of the uncorrected random ADCs with $\hat{x} = \hat{x}_{\text{standard}}$ (1) as a function of σ. It is obvious that such converters are useless unless σ is small.

The corresponding numbers for the corrected ADCs with $\hat{x} = \hat{x}_{\text{corr}}$ (2) are shown in Fig. 2. Also shown in Fig. 2 are the best 10 percentiles and the worst 10 percentiles.

As claimed, the loss in effective resolution due to the threshold errors is bounded to about 1 bit.

Measured results with actual chips confirm this insensitivity to mismatch [3].

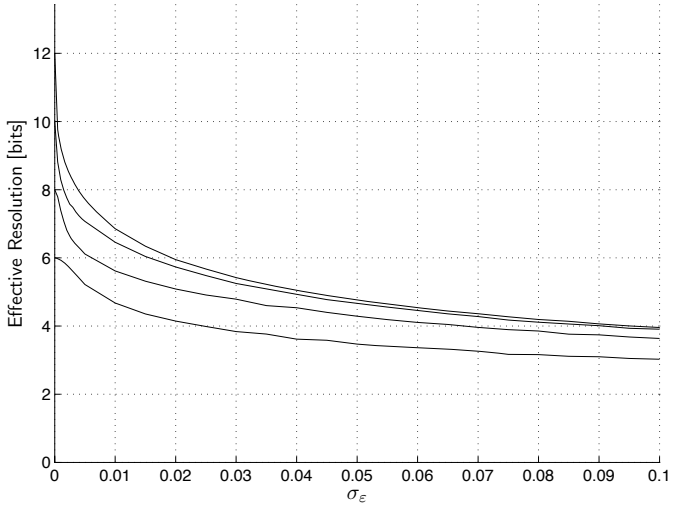

Fig. 1. Average effective resolution vs. σ for uncorrected ADCs with random comparator thresholds.

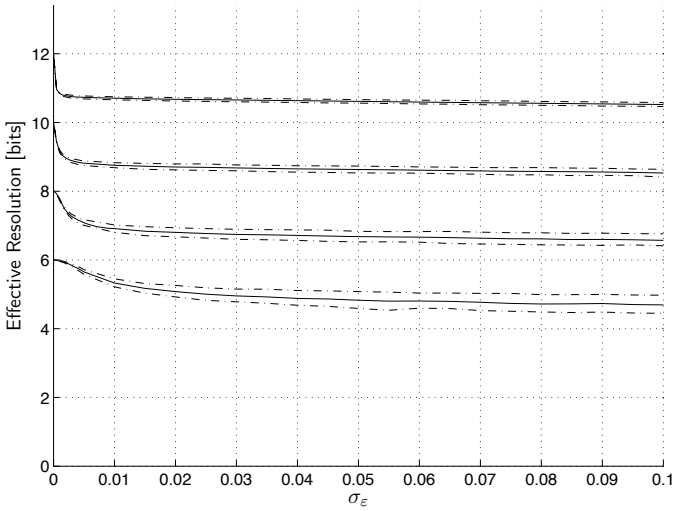

Fig. 2. Effective resolution vs. σ for digitally corrected ADC with random comparator thresholds (same thresholds as in Fig. 1). Solid lines: average effective resolution. Dashed lines: the best 10 percentiles and the worst 10 percentiles.

III. Issues with ADC Correction

We briefly mention some issues with the correction scheme of Section II.

Performance measures beyond MSE: both the linearity and the spectral distortion of the correction (2) are excellent [3].

Correction by look-up table: The quantity $\hat{x}_{\text{corr}}$ (2) as a function of k_{L} can be stored in a look-up table. High precision for $\hat{x}_{\text{corr}}$ is not required [3].

Calibration: The quantities θ_k must be measured. This could be done, for example, by applying a ramp signal $x(t)$ to the converter input and measuring the switching times of all comparators.

Computation of $k_{\text{L}}(x)$ (or of some equivalent quantity) is required for every sample. This is a well-known issue with all flash ADCs, but it is exacerbated by the non-monotonicity of "random" thresholds.

IV. Current Steering DACs with Low-Precision Unit Current Sources

A current steering DAC consists of N current sources that produce the constant currents $c_1, \ldots, c_N$. These current sources are individually switched to form the output current

$$y = \gamma \sum_{n=1}^{N} s_n c_n \tag{4}$$

with $s_n \in \{+1, -1\}$ and with some scale factor γ. (In an alternative version, we have $s_n \in \{0, 1\}$.)

Let $\mathcal{C}$ be the set of all possible output currents (4) for fixed $c_1, \ldots, c_N$ and fixed γ. In an ideal binary-scaled m-bit current steering DAC, we have $c_n = 2^{n-1}$ and $\mathcal{C} = \mathcal{C}_{\text{ideal}}$ with

$$\mathcal{C}_{\text{ideal}} = \gamma\{\pm 1, \pm 3, \pm 5, \ldots, \pm(2^m - 1)\}. \tag{5}$$

Note that the same set $\mathcal{C}$ is obtained with $N = 2^m - 1$ unit current sources $c_1 = c_2 = \ldots = c_N = 1$. However, in this paper, we allow arbitrary current sources c_n and correspondingly general sets $\mathcal{C}$.

In the most straightforward circuit realizations of current steering DACs, the relative cost (both in chip area and in power consumption) of the individual current sources $c_1, \ldots, c_N$ is proportional to their current c_n. (The cost also depends, of course, on the required precision.) If $c_2 = 2c_1$, it is quite correct to think of current source 2 as two copies of current source 1 connected in parallel. In this rough analysis, the cost of the mentioned ideal binary-scaled m-bit DAC (with $c_n = 2^{n-1}$) equals the cost of $2^m - 1$ unit current sources. (As we have seen, a DAC with $N = 2^m - 1$ unit current sources achieves the same resolution as an ideal m-bit DAC.) However, as we shall see below, essentially the same resolution can be achieved with as few as $m + 2$ *imprecise* nearly-unit current sources.

Let x be the real number (available in digital form) that is to be converted into the analog output y according to (4). The conversion may be described as follows:

1) Round x to the nearest point in $\mathcal{C}$.
2) Set the switches $s_1, \ldots, s_N$ accordingly.

For an ideal m-bit DAC, both steps are trivial; for general current sources $c_1, \ldots, c_N$ (and corresponding $\mathcal{C}$), these two steps are the digital correction.

In the following, we will assume $-0.5 \le x < 0.5$. The performance of various DACs will be measured by the mean squared error

$$\text{MSE} = \int_{-0.5}^{0.5} (y(x) - x)^2 \, dx \tag{6}$$

or by the corresponding effective resolution $-\log_2 \sqrt{12\,\text{MSE}}$. The scale factor γ in (4) will be adjusted to obtain the smallest MSE. (This may result in unused points in $\mathcal{C}$ of magnitude larger than 0.5.)

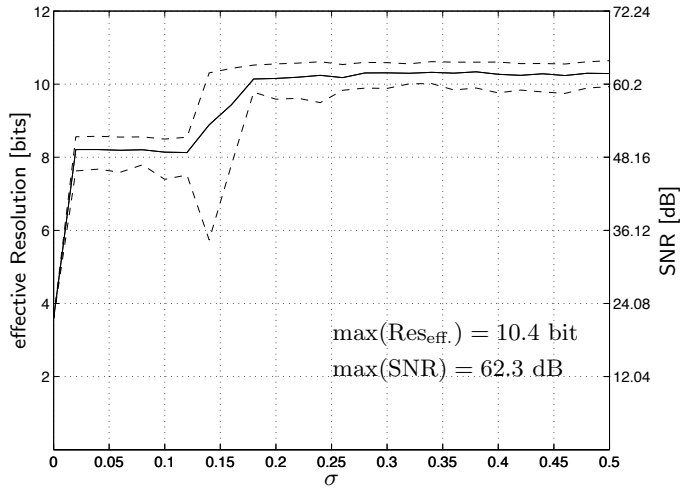

Fig. 3. Effective resolution vs. σ for digitally corrected DAC with $N = 12$ random (nominally unit) current sources. Solid lines: average effective resolution. Dashed lines: 10 best and 10 worst percentiles.

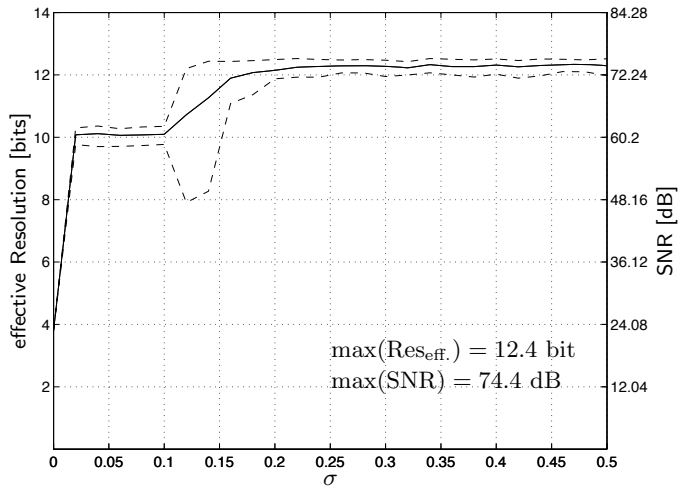

Fig. 4. Effective resolution vs. σ for digitally corrected DAC with $N = 14$ random (nominally unit) current sources. Solid lines: average effective resolution. Dashed lines: 10 best and 10 worst percentiles.

We consider several ensembles of DACs with random source currents $c_1, \ldots, c_N$ given by $c_n = c_{n,\text{nom}}(1 + E_n)$, where $E_1, \ldots E_N$ are independent zero-mean Gaussian random variables with variance σ^2, cf. [2].

In the first ensemble, we use only (imprecise) unit current sources: $c_{n,\text{nom}} = 1$ for all n. The performance of this ensemble as a function of σ is shown in Figures 3 and 4 for $N = 12$ and for $N = 14$, respectively. As is obvious from these figures, the performance of these (corrected) converters is surprisingly good provided that the mismatch (measured by σ) is sufficiently *large*.

In the second ensemble of DACs, we use current sources with nominal currents $c_{n,\text{nom}} = 1.1^{n-1}$. The performance of this ensemble is shown in Figures 5 and 6 for $N = 12$ and for $N = 14$, respectively. With this ensemble, the excellent

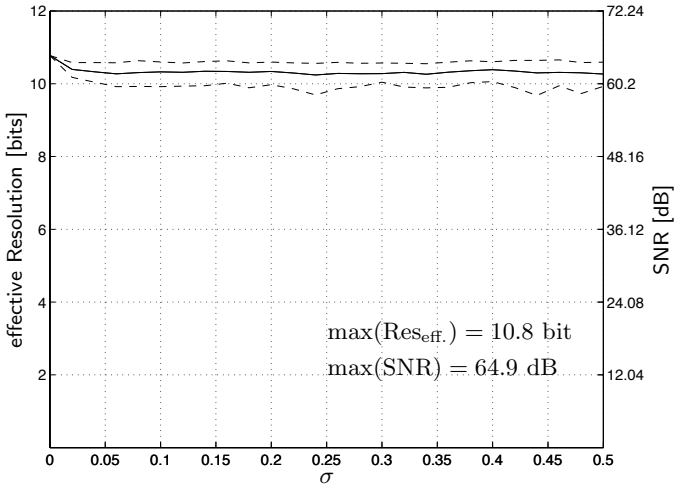

Fig. 5. Effective resolution vs. σ for digitally corrected DAC with $N = 12$ random current sources with mean currents $c_{n,0} = 1.1^{n-1}$, $n = 1, \ldots, N$. Solid lines: average effective resolution. Dashed lines: 10 best and 10 worst percentiles.

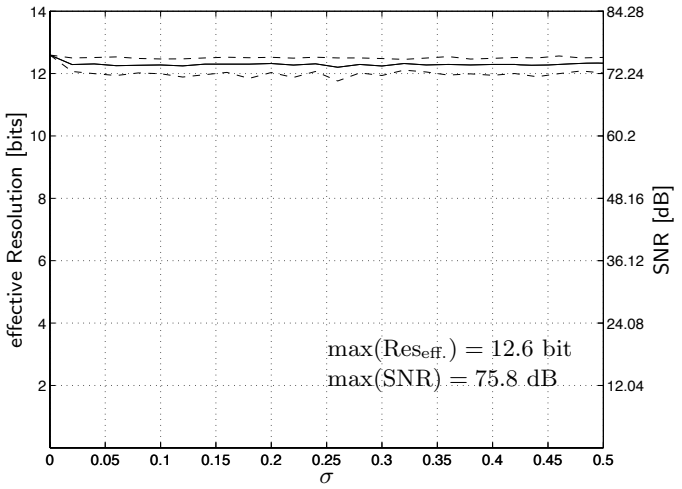

Fig. 6. Effective resolution vs. σ for digitally corrected DAC with $N = 14$ random current sources with mean currents $c_{n,0} = 1.1^{n-1}$, $n = 1, \ldots, N$. Solid lines: average effective resolution. Dashed lines: 10 best and 10 worst percentiles.

resolution of the first ensemble is now achieved at every mismatch level.

In the third and last ensemble of DACs, we use current sources with nominal currents $c_{n,\text{nom}} = 1 + 0.1(n - 1)$. The performance of this ensemble is shown in Fig. 7 for $N = 14$.

In all these examples, we achieve an effective resolution of about $N - 2$ bits with N imprecise current sources.

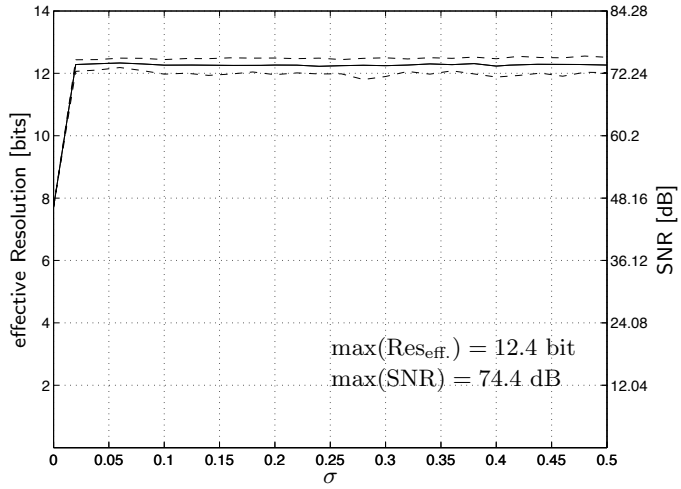

Fig. 7. Effective resolution vs. σ for digitally corrected DAC with $N = 14$ random current sources with mean currents $c_{n,0} = 1 + 0.1(n-1)$, $n = 1, \ldots, N$. Solid lines: average effective resolution. Dashed lines: 10 best and 10 worst percentiles.

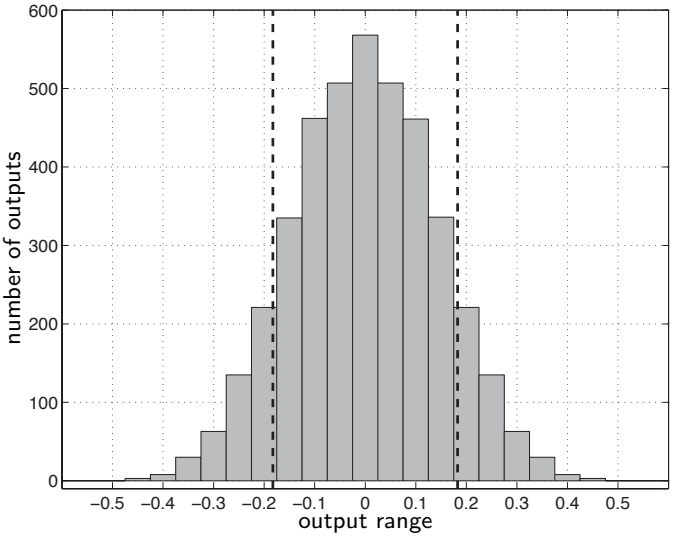

Fig. 8. Distribution of points in $\mathcal{C}$ and used range thereof for the DAC of Fig. 5 with $\sigma = 0.5$.

V. Issues with DAC Correction

We briefly mention some issues with the correction scheme of Section IV.

Performance measures beyond MSE: both the linearity and the spectral distortion are expected to be excellent.

Correction by look-up table: The conversion of the real number x ($-0.5 \le x < 0.5$, available in digital form) into the desired controls $s_1, \ldots, s_N$ of the switches may be carried out as follows. Let m be the effective resolution (in bits) to be achieved. We first round x to, say, $m+2$ bits. From there, we use a look-up table to obtain $s_1, \ldots, s_N$.

Calibration: For any given configuration of switch positions $s_1, \ldots, s_N$, the output current y may be measured by charging a capacitor and measuring the time between two thresholds on the voltage. The calibration can also allow for the case where the output of the DAC is not y as in (4) but some (deterministic) function of it.

Output Range: For "random" DACs, the density of points in $\mathcal{C}$ is higher in the center (around zero) than at the margins. For example, Fig. 8 shows a histogram of the density of points in $\mathcal{C}$ for the DAC of Fig. 5 for ($\sigma = 0.5$). (The central limit theorem may be invoked to argue that the density tends to a Gaussian distribution.) The optimization of the scale factor γ in (4) is therefore important. With an optimized scale factor, only a central region of $\mathcal{C}$ is actually used. In the example of Fig. 8, less than 40% of the total output range (containing over 80% of the points in $\mathcal{C}$) is used.

VI. Conclusions

We have described some basic observations on the effect of component mismatch on the static accuracy of digitally corrected ADCs and DACs. For flash ADCs, the loss of effective resolution due to mismatch is about 1 bit, independently of the mismatch level (unless the mismatch is very small). For current steering ADCs, we have shown that an effective resolution of m bits can be achieved with as few as $m+2$ inaccurate unit current sources. Such corrected DACs may be particulary attractive as components inside ADCs such as, e.g., successive-approximation ADCs or sigma-delta ADCs.

References

[1] E. Balestrieri, P. Daponte, and Sergio Rapuano, "A state of the art on ADC error compensation methods," *IEEE Trans. Instrumentation and Measurement*, vol. 54, no. 4, pp. 1388–1394, August 2005.

[2] J. J. Wikner and N. Tan, "Modeling of CMOS digital-to-analog converters for telecommunication," *IEEE Trans. Circuits and Systems II*, vol. 46, no. 5, pp. 489–499, May 1999.

[3] M. Frey and H.-A. Loeliger, "On flash A/D-converters with low precision comparators," *Proc. 2006 IEEE Int. Symp. on Circuits and Systems*, Toulouse, France, May 14–19, 2006, to appear.