

# On Flash A/D-Converters with Low-Precision Comparators

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**Abstract**— Flash analog-to-digital converters can be built using small (and fast) low-precision comparators with unpredictable thresholds followed by a digital look-up table to correct the output. The look-up table should store digital codes with higher precision than the nominal resolution of the converter. The effective resolution of such a scheme with  $N$  comparators is roughly  $\log_2(N) - 1$  bits. The concept is demonstrated by a chip that achieves almost 7 bit resolution with 256 low-precision comparators.

## I. INTRODUCTION

Analog-to-digital converters (ADCs) are traditionally designed so that all comparators have predictable thresholds close to the thresholds of an ideal uniform quantizer. Such specifications are hard to meet. In particular, limiting the effects of transistor mismatch requires large transistors—“large” by the standards of digital circuits—and large transistors require large currents to achieve high speed.

However, in many applications (e.g., in communications receivers) there is no need for such stringent specifications. All that is really needed is a sufficient density of comparator thresholds; the position of the individual thresholds need not be predictable at design time and may vary substantially from chip to chip. Clearly, an ADC built in this way needs some digital correction. The effective resolution that can be obtained in this way is smaller than the resolution of an ideal uniform quantizer with the same number of thresholds. However, this loss may be more than compensated by the reduced precision requirements in the analog part of the ADC.

ADCs designed (more or less) according to this principle have been reported in [1]–[5]. In all these designs, the ADC contains a bank of low-precision comparators. In [1], a training signal is employed to generate a look-up table that maps the original output codes to a new linearized set. In [2] and [3], only a fraction of the comparators is actually used: during calibration, those comparators with a threshold close to some ideal threshold are identified and the others are deactivated. In [4], all comparators are used and a digital circuit converts the non-monotonic comparator outputs into monotonic digital codes; in this way, an effective resolution of 6 bits (at very high speed) was obtained from 255 low-precision comparators. The mathematical background of optimal ADC post-correction, as well as an example using experimental ADC data are given in [5]. The state of the art of error compensation in ADCs is

summarized in [6].

In this paper, we point out that the effective resolution of suitably corrected ADCs is virtually independent of the comparator mismatch. In consequence, it seems attractive to deliberately use “cheap and dirty” (i.e., small) comparators that are fast without using much power. We illustrate this approach with measurements from an integrated flash ADC with 256 low-precision comparators that achieves an effective resolution of almost 7 bits.

This paper is structured as follows. In Section II, we describe the principle and give some simulation results from a simple model. In Section III, we describe a chip that was actually manufactured, and the corresponding measurements are reported in Section IV.

## II. THE PRINCIPLE

For the sake of concreteness, we will focus on flash ADCs as in Fig. 1 consisting of a bank of “cheap and dirty” (i.e., small) comparators followed by a digital correction.

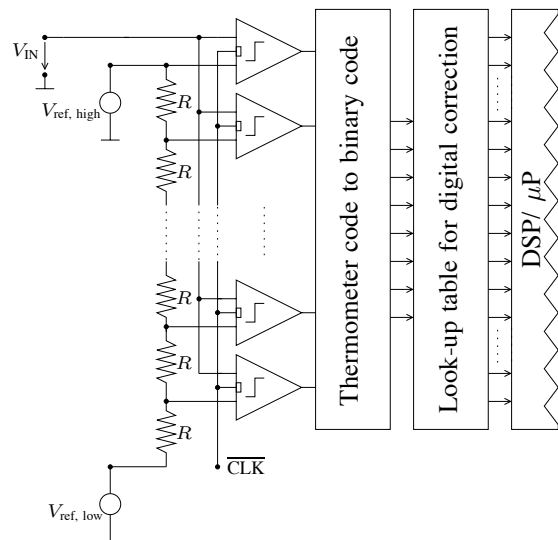


Fig. 1. The complete ADC setup with comparator bank, conversion from a (non-monotonic) thermometer code to a (monotonic) binary code, and the look-up table.

Let  $M$  be an integer and let  $N = 2^M - 1$  be the number of comparators. An ideal uniform quantizer with  $N$  comparators

would thus give a resolution of  $M = \log_2(N + 1)$  bits. The digital correction in our ADC consists of two parts. First, the (non-monotonic) comparator outputs are converted into monotonic digital  $M$ -bit codes (as in [4]). Then follows an  $(N + 1) \times L$ -bit static look-up table that implements a finer correction: for each of the  $N + 1$  quantization bins, the look-up table stores the average of the (measured) upper threshold and the (measured) lower threshold of the bin [7], cf. Fig. 2; this real number is represented by an  $L$ -bit number with  $L > M$ . (As we shall see,  $L = M + 2$  or  $L = M + 3$  will suffice in most cases.)

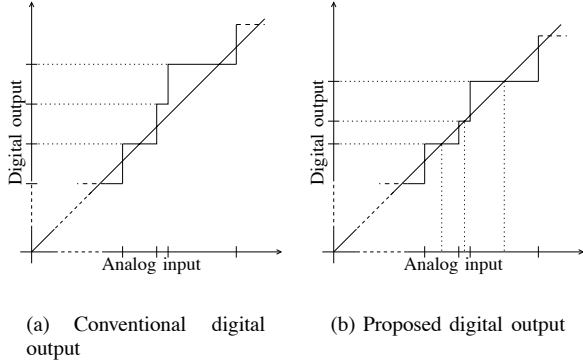


Fig. 2. Input-output characteristics of ADC with comparator mismatch: (a) conventional digital output (digital bins with constant height); (b) proposed digital output.

Obviously, this approach requires measurements of each individual chip. Many ways have been proposed to carry out on-chip calibration of ADCs, e.g., [6], [8]. Although the design of the (analog and digital) circuitry to enable such calibration is not trivial, we will not consider this topic further in this paper.

The performance that can be achieved by such an approach may be obtained from the following simple model. Assume that each comparator threshold is generated randomly by adding a zero-mean Gaussian random variable with variance  $\sigma_\epsilon^2$  to the nominal (ideal) threshold position. (Comparators whose threshold happens to fall outside the nominal range of the input voltage are simply discarded.)

The average performance of such “random” ADCs is shown in Fig. 3. The figure shows the (average) effective resolution (see Eq. 6) as a function of  $\sigma_\epsilon^2$  with the number of comparators ( $2^6$ ,  $2^8$ ,  $2^{10}$ , and  $2^{12}$ ) as a parameter.

As is obvious from Fig. 3, the (average) effective resolution of a properly corrected “random” ADC is virtually independent of the mismatch variance  $\sigma_\epsilon^2$  unless  $\sigma_\epsilon^2$  is very small, i.e., for very large comparators. This means that instead of using the nominal number of high-precision and large comparators for an ADC, twice as many minimum-sized comparators can be integrated to attain a similar effective resolution.

### III. DESIGN EXAMPLE

In order to demonstrate the concept, a flash ADC with 256 comparators was implemented in a 0.25- $\mu\text{m}$  BiCMOS

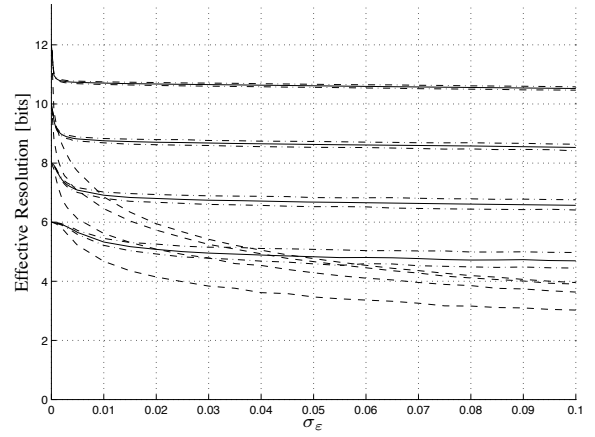


Fig. 3. Average effective resolution of “random” ADCs. Dashed lines: conventional digital output (cf. Fig. 2(a)). Solid lines: proposed digital output (cf. Fig. 2(b)). Dash-dotted lines: 10 and 90 percentiles for proposed digital output.

process (IBM6HP) using only CMOS transistors. The chip was designed for a supply voltage of  $V_{\text{dd}} = 1.8$  V. The chip also contains a 256-to-8 bit multiplexer, but the digital correction is not part of the chip.

The resistor ladder (which generates the reference voltages for the comparators) uses p+ polysilicon resistors; the width of each resistor is  $W_R = 6 \mu\text{m}$  and the length of each resistor is  $L_R = 3 \mu\text{m}$ . The nominal resistance of such a resistor is  $R = 143 \Omega$  and the resistance of the whole ladder is  $R_{\text{ladder}} = 36.6 \text{ k}\Omega$ . The two voltages  $V_{\text{ref, high}}$  and  $V_{\text{ref, low}}$  determine the input range of the ADC; in all our simulations and measurements, we chose  $V_{\text{ref, high}} = 1.5$  V and  $V_{\text{ref, low}} = 0.5$  V. With a voltage difference of 1 V, the current through the ladder is only  $27.3 \mu\text{A}$ .

The comparator circuit (taken from [9]) is shown in Fig. 4. Other than in [9], we use very small transistors (as indicated in Fig. 4). For example, the two input transistors of the differential pair have width  $W_{\text{comp}} = 1 \mu\text{m}$  and length  $L_{\text{comp}} = 0.5 \mu\text{m}$ , which is only slightly larger than the minimum transistor size of the process given by  $W_{\text{min}} = 0.3 \mu\text{m}$  and  $L_{\text{min}} = 0.24 \mu\text{m}$ .

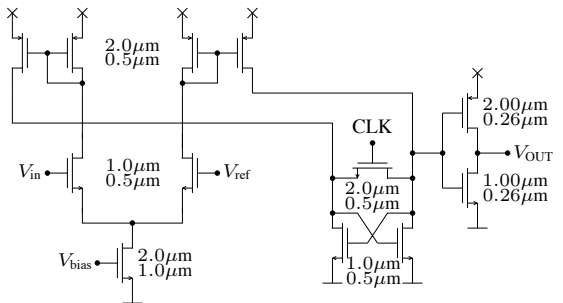


Fig. 4. Schematic of the comparator. The numbers next to the transistors represent the width and the length of the corresponding transistors.

#### IV. MEASUREMENTS

10 chips in DIL-24 packages were available for measurements. The threshold of every comparator was measured with a custom-built measurement device using 12-bit ADCs.

##### A. The Comparators

A statistics for all comparators was compiled. All measured comparator thresholds  $V_{\text{meas},i}$  (with the offset  $V_{\text{ref, low}} = 0.5$  V subtracted) were compared with the thresholds  $V_{\text{threshold},i}$  of the comparators of an ideal 8-bit ADC with an input range of  $\frac{257}{256}$  V. An ideal 8-bit ADC (with 256 comparators) should have comparators switching at the voltages

$$V_{\text{threshold},i} = V_{\text{ref, low}} + (V_{\text{ref, high}} - V_{\text{ref, low}}) \cdot \frac{i}{28}. \quad (1)$$

Table I presents a list of means  $m_\varepsilon$  and standard deviations  $\sigma_\varepsilon$  of the comparators' threshold errors  $\varepsilon_i = V_{\text{threshold},i} - V_{\text{meas},i}$  for each chip separately.

TABLE I  
MEAN  $m_\varepsilon$  AND STANDARD DEVIATION  $\sigma_\varepsilon$  OF THE THRESHOLD ERRORS  
FOR ALL COMPARATORS OF ONE CHIP.

Chip:	$m_\varepsilon$ [mV]	$m_\varepsilon$ [LSB <sub>8</sub> ]	$\sigma_\varepsilon$ [mV]	$\sigma_\varepsilon$ [LSB <sub>8</sub> ]
1	1.29	0.33	14.74	3.77
2	-0.51	-0.13	16.26	4.16
3	-4.65	-1.19	16.36	4.19
4	-0.34	-0.09	15.59	3.99
5	-0.23	-0.06	14.77	3.78
6	-0.70	-0.18	14.91	3.82
7	-1.17	-0.30	15.97	4.09
8	-0.81	-0.21	15.42	3.95
9	-1.29	-0.33	15.64	4.00
10	0.64	0.16	14.84	3.80

The mean and the standard deviation of the threshold errors—expressed in volts as well as in LSBs (1 LSB<sub>8</sub> =  $2^{-8} \cdot (V_{\text{ref, high}} - V_{\text{ref, low}}) = \frac{1}{256}$  V  $\approx$  3.91 mV)—of the comparators over all chips amount to

$$m_\varepsilon = -0.78 \text{ mV} = -0.20 \text{ LSB}_8 \quad (2)$$

$$\sigma_\varepsilon = 15.51 \text{ mV} = 3.97 \text{ LSB}_8. \quad (3)$$

Note that, according to a popular rule of thumb,  $\sigma_\varepsilon \leq \frac{1}{6}$  LSB is required in order to achieve a reasonable yield with an uncorrected ADC [10]. From (3), the accuracy of our converters would thus be adequate for a 4 bit converter. From Fig. 3 (with  $\sigma_\varepsilon = 0.0155$ ), however, we can expect our chips to yield an effective resolution of about 7 bits, which will be confirmed below.

The statistics of the offset voltages of all comparators for each chip separately, as well as for all chips together, are shown in Fig. 5. The Gaussian curves with the mean and standard deviation taken from (2) and (3) are plotted for reference.

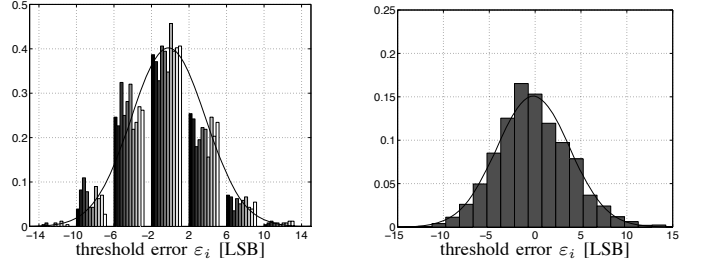


Fig. 5. Distribution of threshold errors. Left: all 10 chips individually. Right: all 10 chips together.

##### B. The Complete ADC

For each chip, the digital correction (which is not part of the chip) was carried out as follows.

- The comparators were rearranged in order to have a monotonic output.
- Gain correction and offset correction was applied, resulting in an ADC with the first comparator switching at an input voltage of  $V_{\text{in}} = 2^{-8}$  V, the last one at  $V_{\text{in}} = 1$  V. The input range of the ADC was defined as  $[0 \text{ V} \dots \frac{2^8+1}{2^8} \text{ V}]$ .
- The mean value of each bin was identified and stored in a correction table as described in Section II.

For comparison, the (conventional) uncorrected digital output was also recorded. For Chip 4, the chip with the worst characteristics, both the calibrated (as in Fig. 2(b)) and conventional (as in Fig. 2(a)) input-output characteristics and quantization error spectrums are plotted in Figs. 6 and 7, respectively.

As in Section II, we will measure the performance of the ADCs in terms of their effective resolution, c.f. (6). (It should be noted that the popular “differential nonlinearity” (DNL) and “integral nonlinearity” (INL), which describe the deviation of the thresholds from their ideal positions, do not appear to make sense for our ADCs.)

The effective resolution is defined as usual. First, let  $Q$  be the rms quantization error, which is defined by

$$Q^2 \triangleq \text{average over whole input range of} \\ ((\text{analog input}) - \text{DAC}_{\text{ideal}}(\text{digital output}))^2. \quad (4)$$

Recall that the rms quantization error of an ideal ADC with bin width LSB is

$$Q_{\text{ideal}} = \frac{\text{LSB}}{\sqrt{12}}. \quad (5)$$

Solving for LSB and assuming that the input range is 1 V, the effective resolution  $\text{Res}_{\text{eff}}$  is then given by

$$\text{Res}_{\text{eff}} = -\frac{\log(\sqrt{12}Q)}{\log(2)} \quad (6)$$

The effective resolution of all 10 chips is listed in Table II. Also shown in Table II is the rms quantization error  $Q_{\text{calib}}$  of the ADC with corrected digital output, as well as the rms quantization error  $Q_{\text{raw}}$  of the ADC with conventional

TABLE II

THE RMS QUANTIZATION ERROR AND EFFECTIVE RESOLUTION.

Chip:	$Q_{\text{raw}}$ [LSBs]	$Q_{\text{calib}}$ [LSBs]	eff. Res. [bits]
1	1.97	0.64	6.84
2	5.49	0.67	6.79
3	4.63	0.72	6.68
4	5.99	0.65	6.83
5	3.85	0.64	6.85
6	4.51	0.57	7.01
7	4.29	0.60	6.95
8	4.83	0.63	6.86
9	3.08	0.58	6.99
10	5.86	0.60	6.94

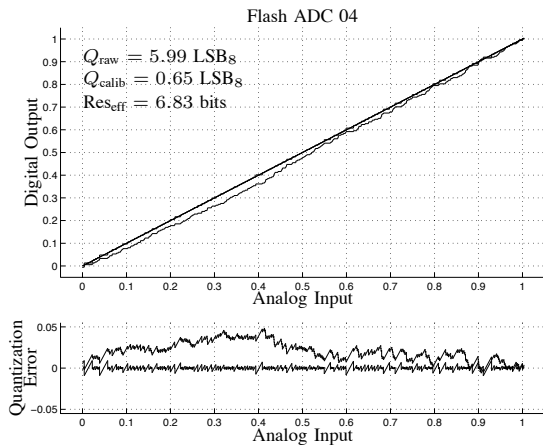


Fig. 6. Top: Input-output characteristics of the ADC chip 4, both conventional and corrected. Bottom: Quantization error of the ADC with conventional and corrected output.

uncorrected digital output. Note that the effective resolution varies from chip to chip, but is close to 7 bits for all 10 chips.

The effective resolution in Table II is based on a digital correction table with full measurement precision. In Table III, the effective resolution (of chips 1 and 2) is shown for a (corrected) digital output using  $L = 8, 9, \dots, 12$  bits. Note that  $L = 10$  suffices to essentially get the maximum possible effective resolution.

TABLE III

THE RMS QUANTIZATION ERROR FOR A DIGITAL OUTPUT WITH  $L = 8 \dots 12$  BITS.

Chip:	$Q_{8b}$	$Q_{9b}$	$Q_{10b}$	$Q_{11b}$	$Q_{12b}$	$Q_{\text{calib}}$
1 [LSBs]:	0.70	0.66	0.65	0.64	0.64	0.64

## V. CONCLUSION

There is an increasing awareness that A/D-converters can be built using low-precision comparators with “random” thresholds. We have pointed out that—nearly independent of the comparators’ mismatch—the effective output resolution of the calibrated ADC is only approximately 1 bit worse than the

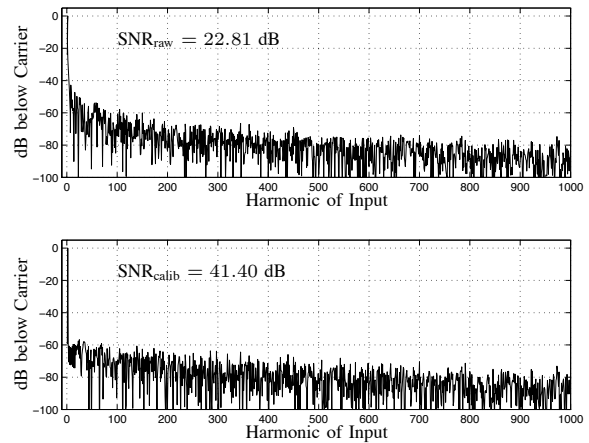


Fig. 7. Quantization error spectrum for the uncalibrated (top) and calibrated flash ADC chip 4 assuming ideal sampling.

output resolution of an ADC with high-precision comparators. The digital correction of such converters should produce the mean value of each quantization bin (which is a real number), or some adequate approximation thereof. As an example, we presented a chip with 256 low-precision converters that achieves a static precision of almost 7 bits.

## VI. ACKNOWLEDGMENTS

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