ANALOG-DECODER EXPERIMENTS WITH SUBTHRESHOLD CMOS SOFT-GATES

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ABSTRACT

A collection of analog "soft-gate" CMOS ASICs operating in subthreshold-mode was implemented in a low-cost semi-custom 0.8 μm technology. These soft-gates allow, in particular, the realization of various decoders for simple error correcting codes on the breadboard level. Measurement results are presented for an (8,4,4) Hamming code.

1. INTRODUCTION

In 1998, Hagenauer [1, 2] and Loeliger et al. [3] independently proposed to decode error correcting codes by novel analog electronic networks; these networks are a direct translation of the Tanner graph [4] or factor graph [5] of such codes into networks of electronic "probability gates" or "soft-gates". More complete accounts on these new analog decoders were given in [6] and [7, 8]; see also [9].

Since 1998, much effort has been spent towards turning these ideas into working chips. The first fully functional analog decoder of this type was built in 1998 by Lustenberger et al. using discrete transistors [8]. Lustenberger et al. then designed and manufactured first, a decoder for a four-state tailbiting (18,9,5) convolutional code and later, a decoder for a (44,22,8) low density code, both in 0.8 μm BiCMOS technology [8, 10]; unfortunately, both of these chips turned out to have some problems with the interface circuits (outside the actual decoder). Hagenauer et al. have demonstrated a perfectly working decoder for a two-state (16,8,3) tail-biting convolutional code in 0.25 μm BiCMOS technology. Winstead et al. [11] have fabricated a decoder of the (8,4,4) Hamming code in 0.5 μm CMOS technology; that decoder, too, was reported to have some minor design error. Xotta et al. have recently announced an ambitious design of a complete turbo decoder for magnetic recording [12], but that chip has not yet been manufactured.

In this paper, we report on a more modest achievement. We have built a series of probability gates as individual CMOS ASICs that allow the realization of various analog decoders on the breadboard level. In particular, we will report measurement results for a decoder of the (8,4,4) Hamming code. That decoder works very well and appears to be surprisingly immune against transistor mismatch.

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2. CODES AND GRAPHS

Error correcting codes are an essential element of most modern communication systems. The invention in 1993 of "turbo coding" and the rediscovery of "low-density parity check codes" have now led to practical codes and decoding schemes which, for most practical purposes, essentially achieve the theoretical performance limits predicted by Shannon's information theory [13]. A natural way of looking at all such codes is by graphical models ("Tanner graphs," "factor graphs"), and the decoding of such codes may be viewed as applying the general iterative "sum-product algorithm" to such graphical models [4, 5].

A Forney-style factor graph (called "normal graph" in [14]) for the (8,4,4) extended Hamming code is shown in Figure 1. The nodes represent either equality constraints or parity-checks. The bits $u_0 \dots u_3$ in Figure 1 will be called "information bits" and the bits $x_4 \dots x_7$ will be called "parity bits". For details, we refer to [14].

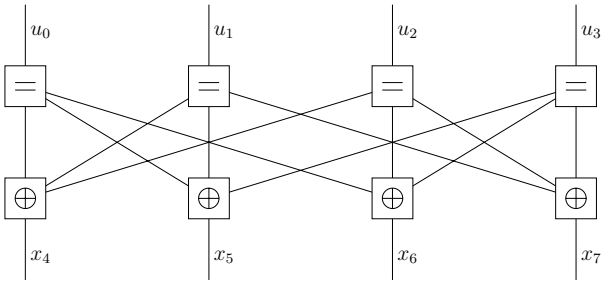

Figure 1: A Forney-style factor graph for the (8,4,4) extended Hamming code.

Any factor graph (or Forney-style factor graph, as e.g., in Figure 1) may be interpreted as a blueprint for a decoder of the corresponding code. In this interpretation, each node of the graph may be viewed as a "processor". The decoder operates by passing "messages" along the edges of the graph; the messages are iteratively (re-)computed by the nodes/processors according to the rules of the sum-product algorithm [5, 14].

Note that the graph of Figure 1 is far from unique. In general, a huge variety of different graphs exists for the same code, and each such graph yields a different decoder.

3. PROBABILITY GATES AND ANALOG DECODERS

As presented in [3], a factor graph such as shown in Figure 1 may be immediately translated into an analog electronic network. The nodes/processors are translated into "probability gates", which are wired together according to the topology of the graph. These probability gates perform computations with probabilities. The circuits rely on the exponential characteristics of either bipolar junction transistors or CMOS transistors operating in the subthreshold region; within the validity of the exponential model, the probability calculations are exact. For details see [7, 8].

We have a collection of over 140 soft-parity-check gates (soft-XOR gates) and just as many soft-equality-constraint gates (soft-EQU gates), each as an individual ASIC in its own package. Each gate has three bidirectional ports. For each of its three output ports, the softXOR gate computes

$$\begin{bmatrix} p_{\mathrm{out}}(0) \\ p_{\mathrm{out}}(1) \end{bmatrix} = \begin{bmatrix} p_{\mathrm{in1}}(0)\, p_{\mathrm{in2}}(0) + p_{\mathrm{in1}}(1)\, p_{\mathrm{in2}}(1) \\ p_{\mathrm{in1}}(0)\, p_{\mathrm{in2}}(1) + p_{\mathrm{in1}}(1)\, p_{\mathrm{in2}}(0) \end{bmatrix} \quad (1)$$

and the softEQU gate computes

$$\begin{bmatrix} p_{\mathrm{out}}(0) \\ p_{\mathrm{out}}(1) \end{bmatrix} = \gamma \begin{bmatrix} p_{\mathrm{in1}}(0)\, p_{\mathrm{in2}}(0) \\ p_{\mathrm{in1}}(1)\, p_{\mathrm{in2}}(1) \end{bmatrix}, \quad (2)$$

where the scale factor γ is implicitly defined by the condition $p_{\mathrm{out}}(0)+p_{\mathrm{out}}(1) = 1$. As described in [7], probabilities are represented by currents. The transistors operate in subthreshold mode, typically at a current-level of about 1 μA, i.e., 1 μA corresponds to probability 1.

The circuits are implemented in a 0.8 μm N-well silicon gate CMOS process (Philips C175SC) using the inexpensive semi-custom mixed-signal array "MD300" provided by Microdul AG, Zürich. The circuit topologies of the two probability gates are described in [8]. Special care was taken to minimize the mismatch of corresponding transistors in current mirrors and differential pairs: 24 unit-transistors were connected in a parallel and interleaved manner ($W_{N,P} = 24 \times 6$ μm $= 144$ μm, $L_{N,P} = 5.6$ μm) to form a common-centroid layout [15]. The NMOS- and PMOS-transistors were sized equally.

This collection of soft-gates allows us to carry out a large variety of measurements. First we can examine the characteristic of a single soft-gate. We then have the possibility to build decoders for different codes. For each code there exists a large family of suitable decoder structures (which we call realizations). Once we have wired one such realization on the breadboard, the impact of transistor mismatch can be analyzed by plugging different sets of ASICs into the sockets. In addition, the influence of some other conditions (e.g. supply voltage, decoder settling time) on the decoder's performance can be studied.

In this paper we present results obtained from the decoder realization for the (8,4,4) extended Hamming code shown in Figure 1. A picture of the assembly is shown in Figure 2. From that figure, it might seem doubtful whether such a decoder can work at all; in fact, we have observed quite robust behavior, as will be detailed below.

4. MEASUREMENT RESULTS

All measurements were carried out on our lab's own measuring device, which contains 16 12-bit D/A- and A/D-converters. The soft-gates' characteristics were verified first: 50 bidirectional softEQU gates as well as 50 bidirectional softXOR gates were measured and simulated. (One fully bidirectional soft-gate contains three unidirectional soft-gates.) The results are shown in Figure 3 for the softEQU gates and in Figure 4 for the softXOR gates. The solid lines represent the ideal characteristics of the soft-gates, whereas the dashed lines show the 10 and 90 percentiles for the 3×50 measured characteristics (i.e. 80 percent of the measurements lie between the dashed lines).

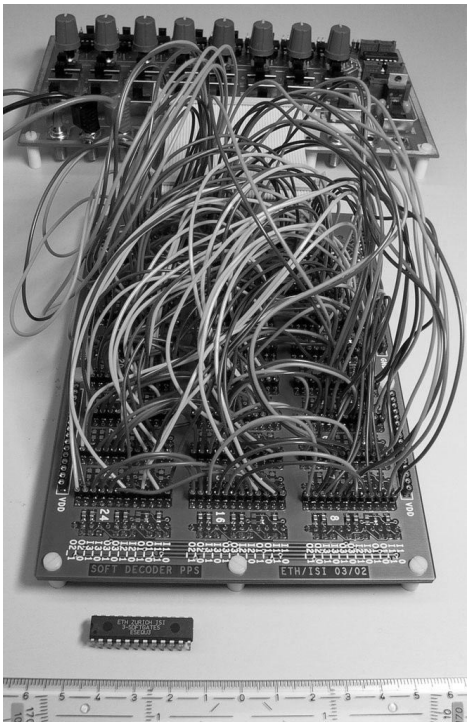

Figure 2: Breadboard-level decoder with a soft-gate chip.

The variations in the soft-gates' characteristics are primarily due to transistor mismatch (and to some degree also due to asymmetries among the circuits); some deviation from the ideal characteristic is also due to the deviations of the real transistors from our exponential model. The flattening of the curves for large log-likelihood ratios of the output of the softEQU gate, as seen in Figure 3, is probably an artifact caused by the resolution limit of the measurement equipment.

Error rate curves were measured both for the binary symmetric channel (BSC) and for the additive white gaussian noise (AWGN) channel. The transmission over the noisy channel was simulated in software, and the resulting "noisy" codewords were applied in parallel to the decoder; after a fixed and preset time the A/D-converters then measured the decoder's outputs. The plots in this paper were obtained with a settling-time of 50 ms.

The effect of transistor mismatch was studied by plugging in 11 different chip sets (all stemming from the same wafer) into the sockets of the decoder shown in Figure 2. For the AWGN channel, 10 error-rate curves were measured up to an SNR of 6 dB; one measurement (which nearly took 2 weeks!) was measured up to an SNR of 8 dB. The results of these measurements are summarized in Figure 5, which shows both the block error rate (which includes

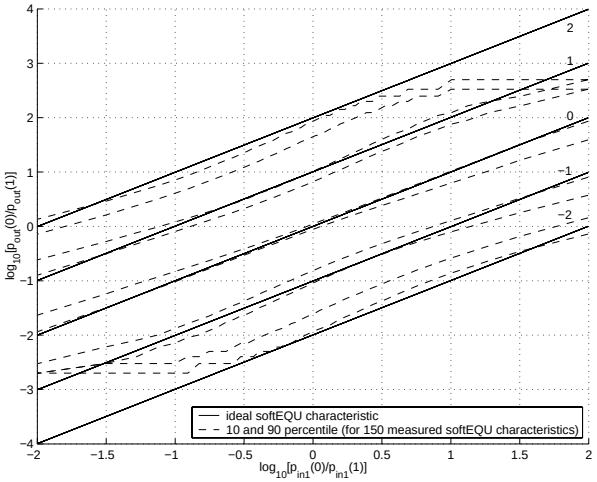

Figure 3: Ideal and measured (10 and 90 percentile, 150 measurements) characteristics of the softEQU gate. The varying parameter is the log-likelihood ratio of the second input: $\log_{10}[p_{in2}(0)/p_{in2}(1)]$.

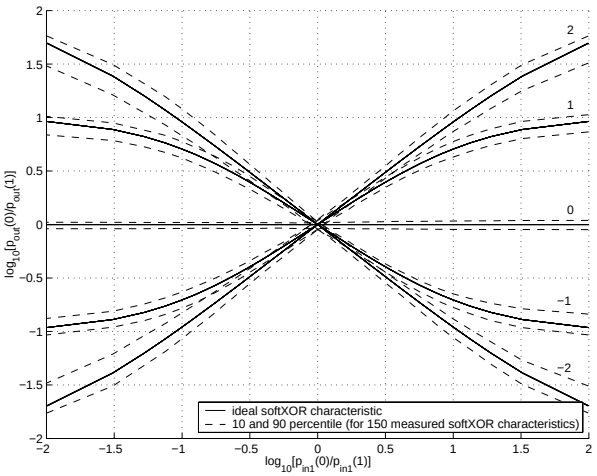

Figure 4: Ideal and measured (10 and 90 percentile, 150 measurements) characteristics of the softXOR gate. The varying parameter is the log-likelihood ratio of the second input: $\log_{10}[p_{in2}(0)/p_{in2}(1)]$.

errors both in the information bits and in the parity bits) and the average information-bit error rate. Also shown in Figure 5 are the corresponding curves for an "ideal" analog decoder with ideal soft-gates according to (1) and (2). (Since the graph of Figure 1 has loops, that ideal analog decoder is not a MAP decoder of the code.) Somewhat surprisingly, the measured performance curves of different chip sets are almost identical; the influence of transistor mismatch, which appears to be quite significant in Figures 3 and 4, is hardly noticable in the overall decoder performance.

The error-rate curves of 10 measured decoders for the BSC are shown in Figure 6. The BSC is obtained as a quantized AWGN

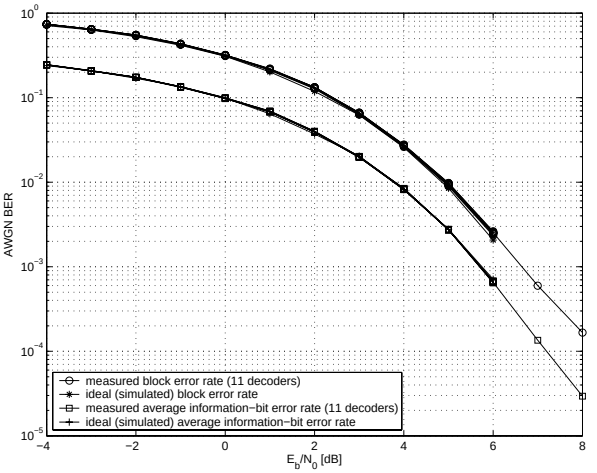

Figure 5: Measured block error rate and measured average information-bit error rate of 11 versions (each with a different set of ASICs) of the decoder of Fig 1 for the AWGN channel. Ideal block error rate and ideal average information-bit error rate for such a decoder.

channel and parameterized by the SNR of the AWGN channel. Independent of the actual SNR, the decoder was operating with a fixed SNR of 6 dB, which was experimentally found to give the best results. As Figure 6 shows, the measured information-bit error rates lie all on top of each other and agree with that of the ideal analog decoder. In contrast, some of the measured block error rate curves (which include errors in the parity bits) are markedly worse than those of the ideal analog decoder. It appears that the parity bits are more sensitive to transistor mismatch than the information bits.

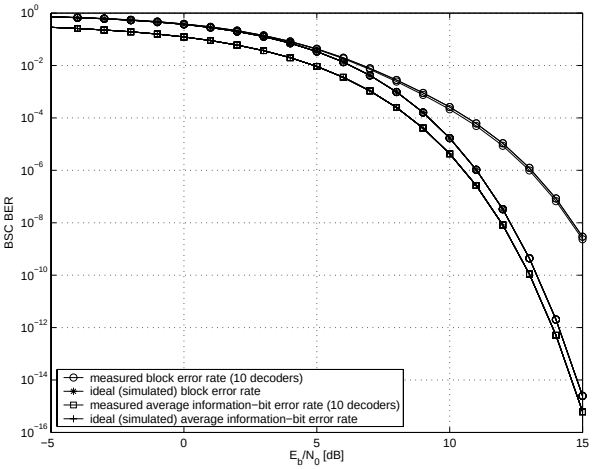

Figure 6: Measured block error rate and measured average information-bit error rate of 10 versions (each with a different set of ASICs) of the decoder of Fig 1 for the BS Channel with a fixed optimal SNR $= 6$ dB. Ideal block error rate and ideal average information-bit error rate for such a decoder.

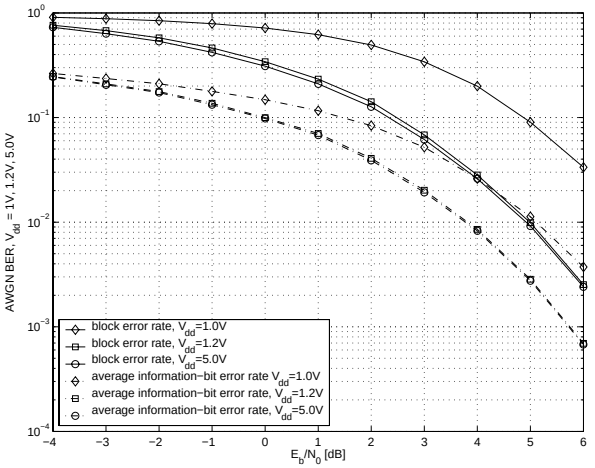

Figure 7: Measured block error rate and average information-bit error rate for the AWGN channel. The supply voltage is adjusted from 5.0 V to 1.2 V and to 1.0 V.

We also experimented with different supply voltages. Again, the circuits proved quite robust. While the circuits were designed for a supply voltage of $V_{dd} = 5.0$ V, the decoder works very well with a supply voltage as low as $V_{dd} = 1.2$ V, as shown in Figure 7.

5. CONCLUSIONS

We have presented measurements of bit error rates and block error rates for an analog decoder implemented with probability gates on the breadboard level. We have observed that the measured overall performance is virtually identical with that of an ideal analog decoder despite of substantial measured nonidealities on the soft-gate level. While the circuits were designed for a supply voltage of 5 V, we have observed no substantial loss of performance when operating them at a supply voltage as low as 1.2 V.

6. ACKNOWLEDGEMENTS

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