Two Experimental Analog Decoders

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ABSTRACT

It has been known for some time that the standard iterative decoding algorithm of turbo codes and similar codes can be mapped directly to simple translinear transistor circuits. However, the experience with such analog decoders is still very limited. This paper presents the architecture and some measurement results for two such decoders: first, a decoder for the (8,4,4) extended Hamming code and second, a decoder for the (16,5,8) Reed-Muller code.

Keywords: *Analog decoder, message passing algorithms, low-power circuits, translinear circuits.*

1 Introduction

Error correcting codes are key components of most modern communication systems. Modern codes such as turbo codes and low-density parity check codes are decoded by the sum-product algorithm or some variation thereof. Such algorithms operate by passing "messages" along the edges of a factor graph of the code [1].

As observed in [2, 3], the sum-product algorithm can be mapped directly into simple analog transistor circuits. In such decoders, the iterations of the standard (discrete-time) decoding algorithm are replaced by the natural (continuous-time) settling behaviour of the transistor network. It is hoped, and partly corroborated by measurements, that such analog decoders consume substantially less power (for a given speed) than a digital implementation of the corresponding iterative decoding algorithm.

A number of experimental chips built according to the principles of [2] and [3] have been presented in, e.g., [4, 5, 6].

Nevertheless, solid experimental results are still scarce. In particular, few systematic measurements of bit error rates, decoding speed, the influence of transistor mismatch and of current density, etc., are available. In this paper, we report such measurements for two different decoders. Decoder 1 is a decoder for the binary (8,4,4) extended Hamming code; Decoder 2 is a decoder for the binary (16,5,8) Reed-Muller code. Both decoders are deliberately "suboptimal" in the sense that their digital (discrete-time) counterpart is iterative and slightly weaker than a maximum-likelihood decoding algorithm.

It should be emphasized that both of these decoders are still toy examples. However, some new ideas were tried in these decoders, and the results of our systematic measurements may be of interest to many researchers in the field.

For the description of our decoders, we use Forney-style factor graphs as in [1].

2 A Decoder for the (8,4,4) Extended Binary Hamming Code

The first decoder of this paper implements the (Forney-style) factor graph of Fig. 1. Since this factor graph has cycles, the standard sum-product algorithm on this graph (and thus also our analog decoder) is not a maximum-likelihood decoder.

The analog decoding network is obtained by implementing the message update rules as analog circuits and connecting these circuits according to the graph topology. The chip layout—annotated with the structure of the decoder—is also shown in Fig. 1.

The circuit consists of the following sub-blocks: current scaling I/O-circuits (with $I_{\text{in}}^{\text{pad}}/I_{\text{in}}^{\text{chip}} = 10$), softXOR gates (parity check nodes) and softEQU gates (equality constraint nodes). The building blocks are implemented as described in [2].

3 A Decoder for the (16,5,8) Binary Reed-Muller Code

The second decoder of this paper implements the factor graph of Fig. 2 (due to Forney [7]).

The factor graph's cycles could be eliminated by considering the super nodes A, B, and C (indicated

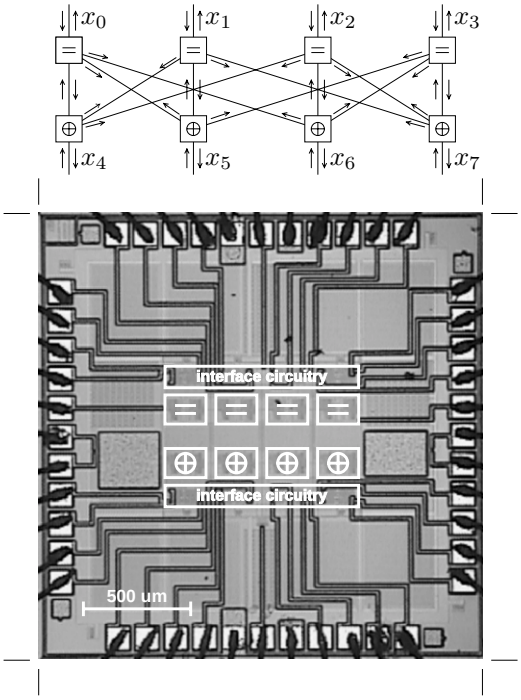

Fig. 1. Factor graph of the Hamming decoder and the corresponding chip.

by the dashed boxes in Fig. 2) and by clustering the variables between these super nodes. The bit-wise MAP estimation is attained by applying the sum-product algorithm to the resulting cycle-free graph and marginalizing the obtained output distributions.

However, we chose to implement a suboptimal algorithm that uses overlapping double-soft-bit messages as illustrated in Fig. 2. The resulting algorithm (which is vaguely related to "generalized belief propagation" [8]) is iterative with some very short feedback loops; for details see [9].

The stability of such nonstandard algorithms is not obvious; indeed, digital (discrete-time) versions of such algorithms usually require heavy damping to work at all. Fortunately, the corresponding analog decoder does not seem to have any problems with stability.

The implemented circuit consists of two main sub-blocks: a serial-to-parallel input interface with analog storage elements and the analog decoder core. The input interface differs from previously published interfaces of analog decoders. It accepts the input messages serially as currents (for this decoder as four currents representing the joint probability densities of two input bits) and stores these currents in parallel by means of the circuit of Fig. 3. In a subsequent

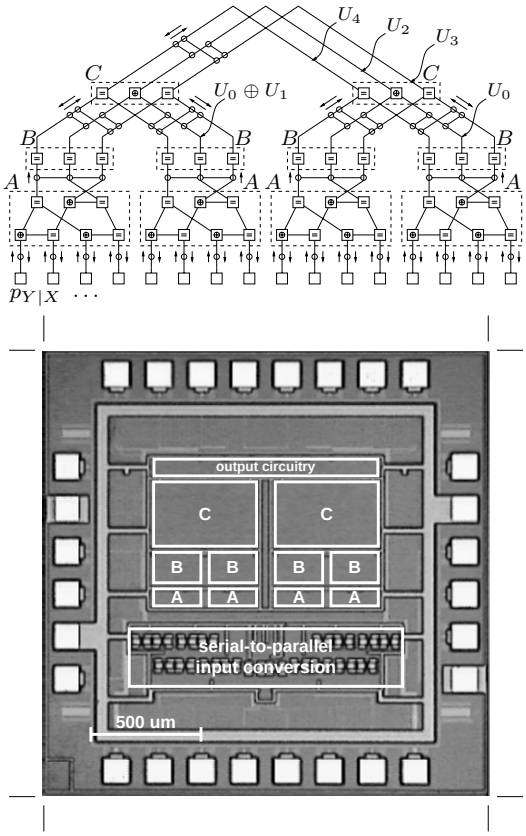

Fig. 2. Factor graph of the Reed-Muller decoder and the corresponding chip.

stage the output currents I_{out} are scaled to the desired unit current. The unit current I_{U} is defined as the current corresponding to a probability of 1.

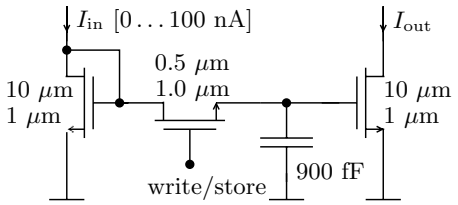

Fig. 3. One slice of the input circuit. The numbers next to the transistors denote their widths and their lengths.

4 Measurements

For both decoders, the bit error rate (BER) and the frame error rate (FER) of 10 different chips under nominal operating conditions are shown in Fig. 4 and Fig. 5, respectively. (We remark that the nominal operating conditions were determined before testing

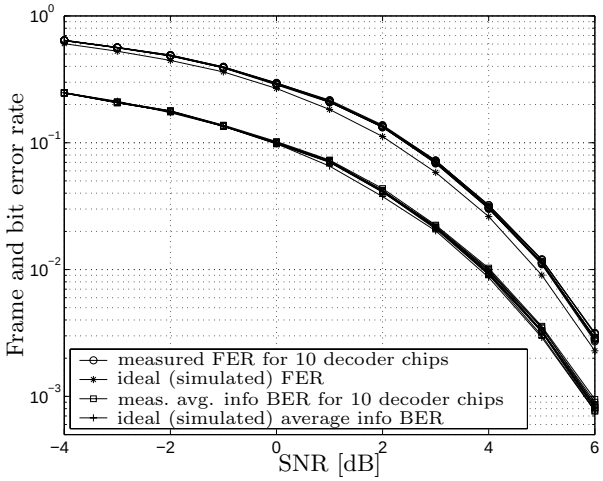

Fig. 4. Measured error rate curves for 10 samples of the (8,4,4) extended Hamming code decoder, along with the corresponding curves obtained by an ideal discrete-time simulation of the algorithm.

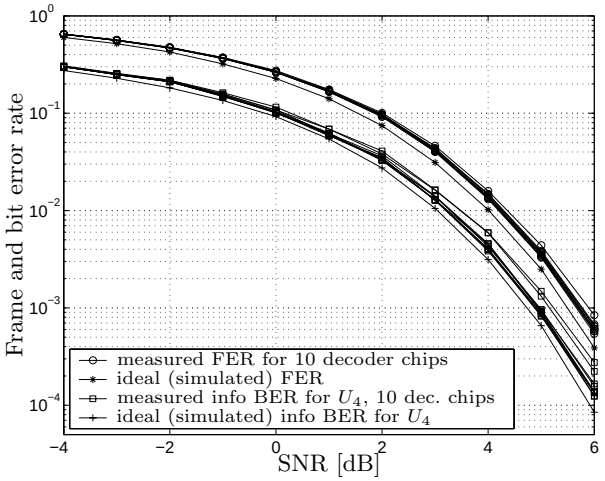

Fig. 5. Measured error rate curves for 10 samples of the (16,5,8) Reed-Muller code decoder, along with the corresponding curves obtained by an ideal discrete-time simulation of the algorithm.

the chip; the best performance is not achieved with these conditions as will be demonstrated in Figs. 8–11 where the chip is tested with increased current level.) For the Hamming decoder the plotted bit error rate is the average bit error rate of the information bits $[x_0 \dots x_3]$; for the Reed-Muller decoder the plotted bit error rate is the error rate of the last information bit u_4, denoted in Fig. 2. The frame error rate includes errors in all the bits. Also shown in Figs. 4 and 5 is the performance of the algorithms obtained by ideal (discrete-time) simulations. As is obvious from the figures, the effect of transistor mismatch is small, but visible.

The curves shown in the following figures allow to estimate the speed of the analog decoders. Figs. 6 and 7 show the error rates of both decoders operating with settling times varying from 100 μs to 100 ms, and from 20 μs to 10 ms, respectively. The settling time, t_{settling}, used as the varying parameter in Figs. 6–9, is defined as the time between the release of the decoder reset and the time the output is sampled.

It can be seen that for the Hamming decoder the performance (with respect to the bit and frame error rates) saturates for $t_{\text{settling}} > 10$ ms and it deteriorates for $t_{\text{settling}} < 1$ ms. The Reed-Muller decoder's performance saturates for $t_{\text{settling}} > 1$ ms and it deteriorates for $t_{\text{settling}} < 100$ μs.

The speed of the analog decoders can be substantially augmented by increasing the unit current, i.e.,

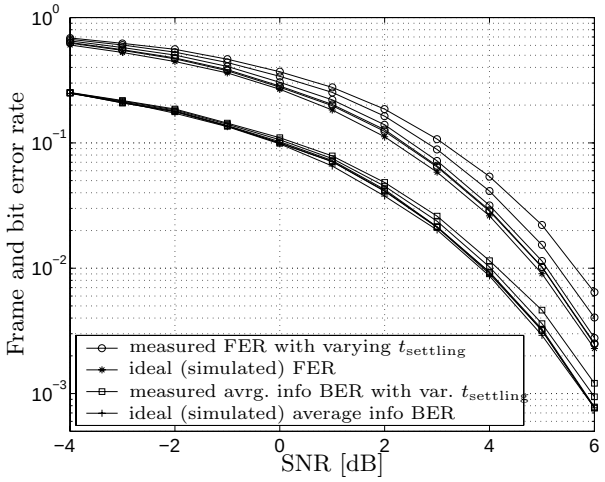

Fig. 6. Measured error rate curves for the (8,4,4) extended Hamming code decoder for varying settling time t_{settling}: 100 μs, 200 μs, 1 ms, 10 ms, 100 ms (resulting in decreasing error rates). The unit current is set to $I_{\text{U}}^{\text{pad}} = 1$ μA.

by operating the transistors in moderate inversion instead of weak inversion. Figs. 8 and 9 show the frame and bit error rate curves for both decoders. For the Hamming decoder chip, no difference in performance is observed for the different settling times t_{settling}; for the Reed-Muller decoder chip, only the curve for a settling time of $t_{\text{settling}} = 20$ μs indicates a slight degradation.

By increasing the unit current the transistors

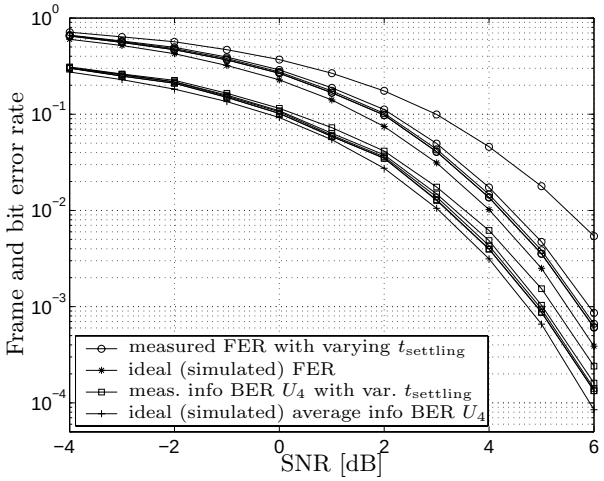

Fig. 7. Measured error rate curves for the (16,5,8) Reed-Muller code decoder with varying settling time t_{settling}: 20 μs, 50 μs, 100 μs, 1 ms, 10 ms (resulting in decreasing error rates). The unit current is set to $I_{\text{U}}^{\text{pad}} = 1$ μA.

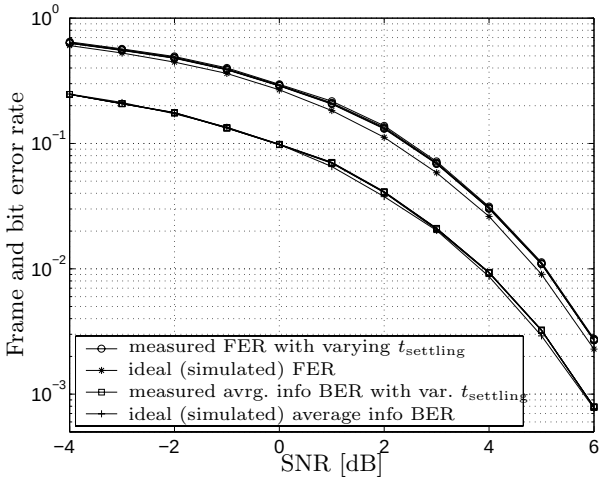

Fig. 8. Measured error rate curves for the (8,4,4) extended Hamming code decoder with varying settling time t_{settling}: 100 μs, 200 μs, 1 ms, 10 ms, 100 ms (resulting in decreasing error rates). The unit current is set to $I_{\text{U}}^{\text{pad}} = 30$ μA.

move away from the weak inversion with its exponential characteristic. The exponential behaviour of the transistors is necessary for obtaining the correct circuit functionality. However, by increasing the current-level, transistor mismatch is reduced. These two opposing effects lead to a trade-off between high current levels (decreased mismatch) and small current levels (better exponential behaviour). As depicted in Fig. 10, we see that for both current levels the error rate performance of the (8,4,4) extended Hamming decoder chip coincides. For the (16,5,8) Reed-Muller decoder chip, the higher current level results in a better performance as is shown in Fig. 11.

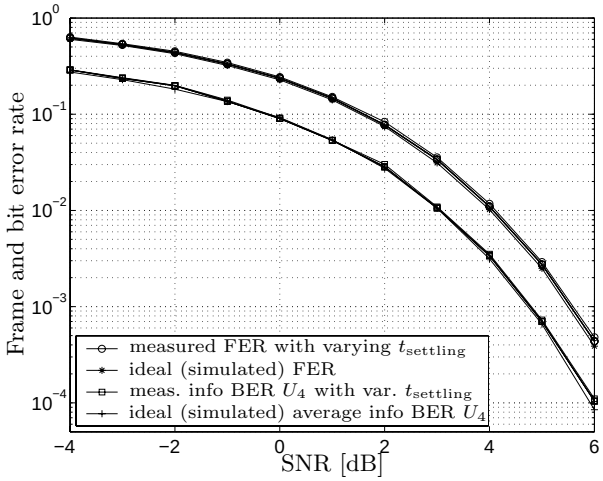

Fig. 9. Measured error rate curves for the (16,5,8) Reed-Muller code decoder with varying settling time t_{settling}: 20 μs, 50 μs, 100 μs, 1 ms, 10 ms (resulting in decreasing error rates). The unit current is set to $I_{\text{U}}^{\text{pad}} = 30$ μA.

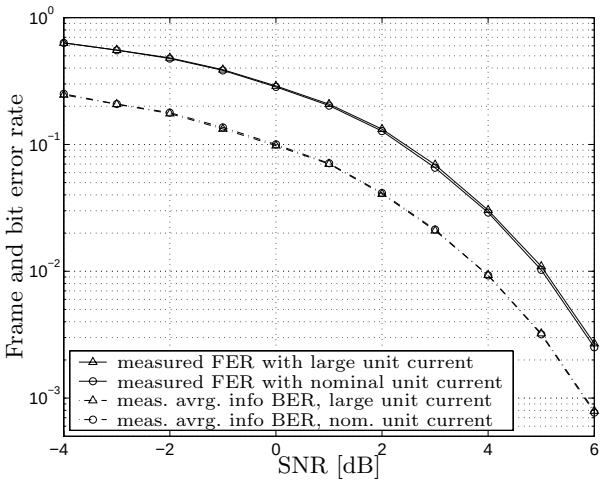

Fig. 10. Measured error rate curves for the (8,4,4) extended Hamming code decoder with large $I_{\text{U}}^{\text{pad}} = 30$ μA and nominal $I_{\text{U}}^{\text{pad}} = 1$ μA unit currents.

Although both decoders were designed for $V_{\text{dd}} = 1.8$ V, the measured bit error rates do not change if the supply voltage is reduced to 0.7 V and 0.9 V, respectively. This is shown in Fig. 12 for the (8,4,4)

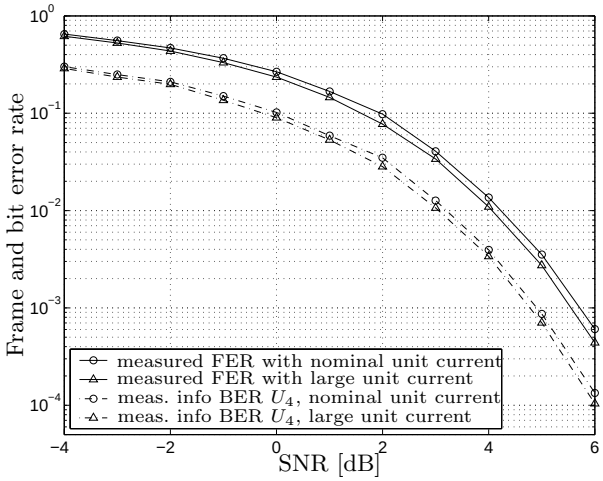

Fig. 11. Measured error rate curves for the (16,5,8) Reed-Muller code decoder with large $I_{\mathrm{U}}^{\mathrm{pad}} = 30\ \mu$A and nominal $I_{\mathrm{U}}^{\mathrm{pad}} = 1\ \mu$A unit currents.

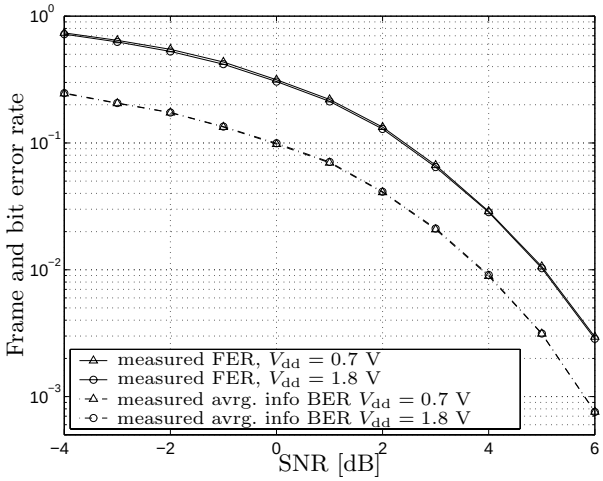

Fig. 12. Measured error rate curves for the (8,4,4) extended Hamming code decoder with low ($V_{\mathrm{dd}} = 0.7$ V) and nominal ($V_{\mathrm{dd}} = 1.8$ V) supply voltage.

extended Hamming decoder chip and in Fig. 13 for the (16,5,8) Reed-Muller decoder chip.

Some key data of both decoders, for nominal conditions ($V_{\mathrm{dd}} = 1.8$ V, $I_{\mathrm{U}}^{\mathrm{pad}} = 1\ \mu$A), are listed in Table 1. It should be emphasized that the chips show better performance (shorter decoding time, lower error rates) by moving away from the nominal conditions by increasing the unit current.

The decoding time t_{dec}, used as a measure for the speed of an analog decoder, is defined as the minimal settling time the decoder needs for attaining

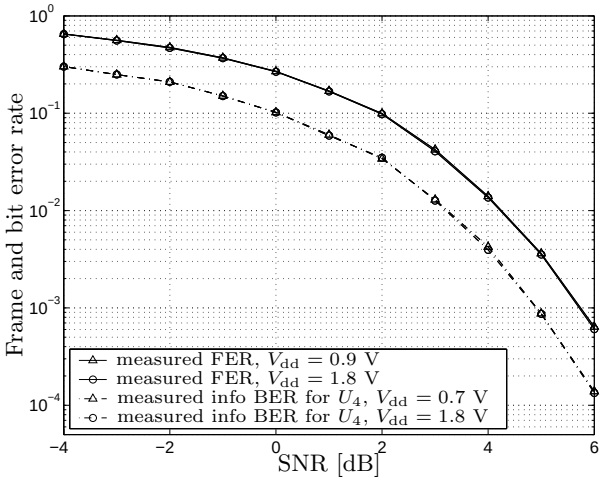

Fig. 13. Measured error rate curves for the (16,5,8) Reed-Muller code decoder with low ($V_{\mathrm{dd}} = 0.9$ V) and nominal ($V_{\mathrm{dd}} = 1.8$ V) supply voltage.

the minimal error rate up to plot accuracy. Applying this definition to the two decoders, the decoding time for the Hamming decoder is $t_{\mathrm{dec}} = 10$ ms, and $t_{\mathrm{dec}} = 1$ ms for the Reed-Muller decoder. (We remark that, in the literature, "decoding time" is sometimes not well defined.)

The power consumption given in Table 1 applies to nominal operating conditions; P_{tot} is the total power (measured) and P_{core} is the power dissipation of the decoder core without the interface.

The "energy per decoded info bit" in Table 1 is defined as $P_{\mathrm{tot}} \cdot t_{\mathrm{dec}}/$(number of information bits).

	(8,4,4) Hamming	(16,5,8) Reed-Muller
Technology:	0.25 μm (IBM6HP)	0.18 μm (IBM7HP)
Die size:	2×2 mm^2	2×2 mm^2
Active area:	0.5×0.7 mm^2	1×0.65 mm^2
nMOS size:	10 μm/ 1 μm	10 μm/ 1 μm
pMOS size:	30 μm/ 1 μm	30 μm/ 1 μm
V_{dd} (nominal):	1.8 V	1.8 V
V_{dd} (minimal):	0.7 V	0.9 V
$I_{\mathrm{U}}^{\mathrm{pad}}$/ $I_{\mathrm{U}}^{\mathrm{chip}}$:	1 μA/ 100 nA	1 μA/ 100 nA
P_{tot}:	55 μW (meas.)	55 μW (meas.)
P_{core}:	$< 5\ \mu$W (sim.)	$< 5\ \mu$W (sim.)
t_{dec}:	10 ms	1 ms
Energy per dec. info bit:	140 nJ (meas.)	11 nJ (meas.)

Table 1. Some key data of the decoder chips.

5 Concluding Remarks

We have presented two new analog decoders in CMOS technology. The first decoder has a rather standard architecture with a parallel interface. The second decoder incorporates an experimental version of an extension of the sum-product algorithm with "overlapping" multi-variable messages and very short feedback loops, as well as a novel serial interface. Extensive measurement results (perhaps the most extensive in the literature so far) were presented for both decoders.

6 Acknowledgments

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