Clockfeedthrough Compensation Technique for Switched-Current Circuits

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Abstract—A new clockfeedthrough compensation scheme for switched-current systems is proposed. The circuit cancels both the signal dependent and the constant clockfeedthrough term. It is shown that this concept can be used to derive various sample-and-hold circuits, depending on the desired clock frequency, accuracy, and power dissipation.

I. INTRODUCTION

A major limitation in switched-current applications is clockfeedthrough (CFT), which is caused by at least one transistor switch connected to a holding capacitor. CFT originates from carriers released from the channel and from coupling of the clock through the gate-diffusion-overlap capacitances of the switch. Due to the square law characteristic of the memory MOS transistor, every signal-dependent error voltage on the gate produces both a signal dependent offset and harmonic distortion of the output current. A number of suggestions have been presented to solve this problem. In general, they propose either the cancellation of only the signal dependent part of the CFT [1], [2], or a reduction of the maximum possible speed of the circuit, e.g., by using algorithmic techniques [3].

II. CFT ANALYSIS

From [4] we know that the charge injected through the MOS switch S in Fig. 1 is given by

\[ Q_{ch} = (V_H - V_{gs} - V_{TS})W_S L_S C_{ox}, \]

where \( V_H \) is the high clock amplitude applied to the switch, \( V_{gs} \) the gate-source voltage of the memory transistor \( M_M \), \( W_S L_S \) the area, and \( V_{TS} \) the threshold voltage of the switch. Depending on the capacitance ratios on each side of switch S, a fraction \( \delta \) of this charge flows into the memory capacitor \( C_M \). A second contribution to the CFT error results from the gate-source-overlap capacitance \( C_{ovs} \) of the switch. The total injected charge into the memory capacitor is

\[ q_{err} = \delta(V_H - V_{gs} - V_{TS})W_S L_S C_{ox} + (V_H - V_L)W_S L_{ovs} C_{ovs}, \]

where \( V_L \) is the low clock amplitude and \( W_S L_{ovs} \) the overlap area on the source side of switch S. The resulting CFT error voltage across the memory capacitor \( C_M \) with the area \( W_M L_M \) is

\[ V_{CFT} = \frac{\delta(V_H - V_{gs} - V_{TS})L_S C_{ox} + (V_H - V_L)L_{ovs} C_{ovs} W_S}{W_M L_M C_{ox}}, \]

Neglecting channel length modulation, the drain current \( I_{ds} \) in phase \( \phi_2 \) can be expressed as (4).

\[ I_{ds} = \frac{\beta}{2}(V_{gs} - V_{TM} + V_{CFT})^2. \]

The resulting output current \( i_o \) can be split into the desired current \( i_{in} \) and an error term \( i_{err} \).

\[ i_{err} = -\frac{\beta}{2}[(V_{gs} - V_{TM})V_{CFT} + V_{CFT}^2]. \]

Thus the error voltage calculated in (3) produces the error current given in (5).

III. PROPOSED COMPENSATION CIRCUIT

The basic idea of our proposed compensation technique is to split the memory transistor \( M_M \) into three equal parts \( M_{11}, M_{12}, M_{13} \) in Fig. 2 and to inject a certain amount of CFT into each one of them by using multiples \( k_j \) \( (j = 1, 2, 3) \) of a switch unit \( (k_j W_S L_S) \) on their gates. It is then possible to compensate for the error current on the output of the memory cell by simply adding the scaled differences of the individual error currents.

The error current for the memory cell in Fig. 2 is given by (6).

\[ i_{err} = -\frac{\beta}{2}\sum_{j=1}^{3}[2k_j V_{CFL}(V_{gs} - V_{T}) + V_{CFT}^2 k_j^2]. \]
TABLE I
SUMMARY OF MEMORY CELL (S/H) COMPARISON

<table>
<thead>
<tr>
<th>Simulations for ( J = 100 \mu A )</th>
<th>Simple S/H</th>
<th>S/H with set (a, b)</th>
<th>S/H with set (c)</th>
<th>S/H with set (d)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Noise level of the cell</td>
<td>30 bits</td>
<td>11 bits</td>
<td>11 bits</td>
<td>11 bits</td>
</tr>
<tr>
<td>Dynamic range limited by noise</td>
<td>6 bits</td>
<td>6 bits</td>
<td>6 bits-(*)</td>
<td>6 bits-(*)</td>
</tr>
<tr>
<td>Switch size ( W = 2/L )</td>
<td></td>
<td>(12 bits-(*))</td>
<td>(14 bits-(*))</td>
<td>(16 bits-(*))</td>
</tr>
<tr>
<td>Power (for ( V_{DD} = 3 \text{ V} ))</td>
<td>0.35 mW</td>
<td>0.8 mW</td>
<td>0.63 mW</td>
<td>0.86 mW</td>
</tr>
<tr>
<td>Active area</td>
<td>0.025 mm(^2)</td>
<td>0.07 mm(^2)</td>
<td>0.06 mm(^2)</td>
<td>0.065 mm(^2)</td>
</tr>
<tr>
<td>Relative max. clock frequency (compared to simple S/H)</td>
<td>1</td>
<td>1/2</td>
<td>1/1.67</td>
<td>1/2.33</td>
</tr>
</tbody>
</table>

The scaled differences of the error currents are given by (7) and (8).

\[ i_{e1} = \frac{\beta}{2} \left[ 2V_{CLF}(V_{gs} - V_T)(k_1 - k_2) + V_{CLF}^2(k_1^2 - k_2^2) \right] \]

\[ i_{e2} = \frac{\beta}{2} \left[ 2V_{CLF}(V_{gs} - V_T)(k_1 - k_3) + V_{CLF}^2(k_1^2 - k_3^2) \right] \]

(7)

(8)

For complete CFT compensation, \( i_{err} + i_{e1} + i_{e2} = 0 \) must hold, which results in (9) and (10).

\[-(k_1 + k_2 + k_3) + \alpha_1(k_1 - k_2) + \alpha_2(k_1 - k_3) = 0 \]

\[-(k_1^2 + k_2^2 + k_3^2) + \alpha_1(k_1^2 - k_2^2) + \alpha_2(k_1^2 - k_3^2) = 0 \]

(9)

(10)

There is an infinite number of solutions for (9) and (10). For practical reasons, it is convenient to choose integers for the \( k_j \) values. For example, a solution set (a) \( \alpha = [\alpha_1, \alpha_2] \) for a given \( k = [k_1, k_2, k_3] \) is \( \{k, \alpha\} = \{(1,2,3), [-10,2]\}\). From a practical point of view, a more interesting solution set (b) is given by \( \{k, \alpha\} = \{(1,2,4), [-7,0]\}\), which eliminates one scaling stage.

Equation (3) shows that each transistor \( M_{2j} \) in Fig. 2 also contributes individually to the error voltage \( V_{CFI} \). With reference transistor \( M_{11} \) (gain factor \( \beta_{11} \)) and an additional gain scaling factor \( \beta_{2j} = \gamma_2j/\beta_{11} \), (11) and (12) replace (9) and (10).

\[-\sum_{j=1}^{3} \frac{k_j}{1 + \gamma_2j} + \alpha_1 \gamma_22 \left( \frac{k_1}{1 + \gamma_22} - \frac{k_2}{1 + \gamma_22} \right) \]

\[+ \alpha_2 \gamma_23 \left( \frac{k_1}{1 + \gamma_23} - \frac{k_3}{1 + \gamma_23} \right) = 0 \]

(11)

\[-\sum_{j=1}^{3} \left( \frac{k_j}{1 + \gamma_2j} \right)^2 + \alpha_1 \gamma_222 \left( \frac{k_1}{1 + \gamma_222} \right)^2 - \left( \frac{k_2}{1 + \gamma_222} \right)^2 \]

\[+ \alpha_2 \gamma_233 \left( \frac{k_1}{1 + \gamma_233} \right)^2 - \left( \frac{k_3}{1 + \gamma_233} \right)^2 \]  

(12)

This results in the solution sets (c) \( \{k, \gamma, \alpha\} = \{(1,2,2), [1,1,0], [-7,0]\}\) and (d) \( \{k, \gamma, \alpha\} = \{(1,1,1), [1,3,0], [2,3,3,0]\}\) for \( \gamma = \{\gamma_{21}, \gamma_{23}, \gamma_{22}, \gamma_{233}\} \). These two sets are of practical interest because the overhead is small. In general, higher values of the \( \gamma_{2j} \)-factors will result in lower \( \alpha \)-values with inferior frequency performance of the memory circuit.

IV. SIMULATION AND RESULTS

The circuit shown in Fig. 2 was simulated with ESPICE and HSPICE, using the 1 \( \mu \)m SACMOS process [5] and the sophisticated transistor charge models MOST and BSIM, respectively. To improve accuracy, regulated cascode current sources and current mirrors were used. The bias current \( J \) was 100 \( \mu \)A and the circuit was operated at a 3 V supply. For a memory transistor with \( W/M = 90/10 \) and a clock frequency of 1 MHz (\( tr_{in} = 10 \) ns) the CFI contribution to the output current was measured for input currents between \(-50\) to \(50 \) \( \mu \)A. For solution set (c) a dynamic range of 14 b and for set (d) 16 b was obtained. This difference can be explained by the better symmetry of the \( \delta \)-factor in (3) with set (d). In real applications noise and transistor mismatch will reduce the dynamic range. The noise level of the proposed memory cell can be calculated as 11 b below the smallest input current [4]. In order to simulate the nonideal matching of the circuit, a Monte Carlo analysis was performed for set (d). With [6], [7] we conclude that the mismatch in the conductance constant of (4) due to edge variation is the dominant source of mismatch in \( \beta \). Taking a standard deviation of mismatch in length and width of 0.01 \( \mu \)m for all \( M_{1j}, M_{2j} \) and switches, a Monte Carlo analysis with 100 runs results in a current variance \( \sigma_i^2/\mu_i \) of 1.5% for the whole input current range. The performance of the proposed circuit improves with larger switch and memory areas. Thus it is ideally suited for memory cells with high transconductance \( g_{mn} \), where a large switch conductance \( g_s \) is needed for rapid settling of the cell.

In order to generate the \( \alpha \)-values, an additional bias current of 0.15J is assumed. Thus, the total current for solution (c) is 1.82 J, and 2.48 J for (d), both of which are at least a factor of 2 less than reported in [1], [2]. The maximum clock frequency for solution (c) is 1.66 times lower than for the one-transistor-solution shown in Fig. 1 and 2.33 times lower than for (d). Thus, depending on the application, a trade-off between speed and accuracy must be made. Table I shows a comparison between the simple memory cell and the compensated versions.

Using these memory cells in a simple integrator configuration [4], some of the additional transistors can be shared. Fig. 3 shows the noninverting lossless integrator for sets (c) and (d) with \( M_{1j} \) and \( M_{2j} \), as memory cells and \( M_{3j} \), as output transistors. In this case the p-channel current-mirrors in the compensation circuit are the same for both memory cells.
V. CONCLUSION

A new scheme for CFT compensation in switched-current circuits has been presented. By using multiples of unit transistors for the compensation, high resolution current memory cells can be built. The resulting circuits provide increased speed capabilities and dissipate less power than circuits previously reported on.

REFERENCES