DESIGN TECHNIQUES FOR HDTV SWITCHED-CURRENT DECIMATORS

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Abstract — **The design of switched-current decimators for wide bandwidth video filtering applications is presented. Applying topologies with only one input commutator to switched-currents allows the design of high speed polyphase input branches with reduced distortion. These concepts were utilized in the implementation of a linear phase 19 tap FIR filter chip with an amplitude response tailored to video applications. It is expected that the prototype filter implemented in a 0.5μm CMOS process will operate at an input sampling rate of 135MHz and with a decimating factor of 5.**

I. Introduction

Video signal processing is a key driver for today's research in analog IC design, mainly because of the rapidly expanding market it represents. Simplicity in the top-level design and full compatibility with digital processes are the key factors leading to cheap IC-chips. Although the main part of present-day signal processing chips is digital, it is in the analogue section in which the most significant performance improvements can be made, mainly in the interface part. For the interfacing between the analogue and the digital parts video systems usually comprise an anti-aliasing filter (AAF) followed by an analogue-digital (A/D) converter (Fig. 1), and from the digital to the analogue domain a digital-analogue (D/A) converter followed by an anti-imaging filter (AIF) [1], [2]. It is well known that it is difficult to design AAF's and AIF's for video applications because of stringent performance limitations due to speed or accuracy requirements [3]. Solutions currently available are based on traditional switched-capacitor (SC) or switched-current (SI) filter structures and include parallelism [4] and double sampling techniques [5] to increase the input sampling rate. However, the output sampling frequency $F_{s,\,out}$ of a filter with signal frequencies $f_{sig} = [0, f_{max}]$ is determined by the Nyquist frequency $F_{s,\,out} \geq 2f_{max}$ and the input sampling frequency $F_{s,\,in}$ is determined by the desired oversampling factor for relaxing the prefiltering requirements, $F_{s,\,in} \gg 2f_{max}$. Therefore, it is necessary to use multirate analog signal processing techniques to substantially reduce the prefiltering requirements and to maximize the speed-accuracy-factor of the filter at the output. By employing multirate FIR filters for AAF and AIF designs, the selectivity of the filter can be made very high. At the same time speed and accuracy conditions are relaxed. Furthermore, to be fully compatible with digital CMOS processes, switched-currents (SI) [6] are advantageously employed. The derived circuits are investigated not only from the topological point of view but also with regard to optimum transistor design.

In this paper we introduce, both analytically and graphically, two new polyphase SI decimator structures employing active-delay-blocks (ADB) to implement the delay lines [7], [8]. We describe a linear phase FIR filter structure with reduced complexity of the input commutator, and an FIR filter for relaxed timing requirements. The latter was implemented and designed for an amplitude response tailored for video interface applications using a 0.5μm CMOS process.

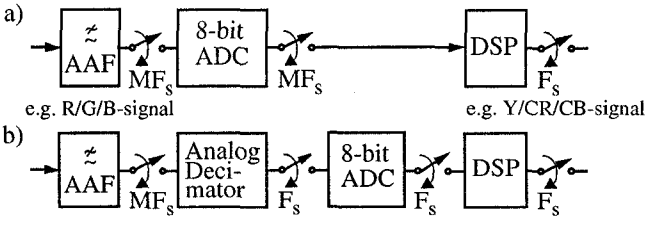

Fig. 1 Video coding system with a) predominantly digital and b) mainly analog architecture.

II. Architecture and Timing

In what follows, the prototype filter is a linear time-invariant FIR filter of order N with the discrete time transfer function

$$H(z) = \sum_{n=0}^{N-1} h_n z^{-n} \qquad (1)$$

where the unit delay period is related to the input sampling frequency $1/MF_s$. The decimating factor M of the polyphase filter was chosen to be such that the speed-versus-accuracy requirement of the basic SI sample-and-hold cell was optimized. For the illustrated examples M is chosen to be 5 and $N = 19$. In this case the selectivity $S = N/M$ is 3.8, which is considerably larger than previously reported [9]. The coefficients h_n of the symmetric impulse response considered here are given in TABLE 1, [8].

TABLE 1 Impulse response coefficients of the FIR decimator

h_1 =-0.00727	h_6 = 0.06020	h_{11} = 0.11294	h_{16} = 0.01537
h_2 =-0.00293	h_7 = 0.08749	h_{12} = 0.11215	h_{17} = 0.00284
h_3 = 0.00284	h_8 = 0.11215	h_{13} = 0.08749	h_{18} =-0.00293
h_4 = 0.01537	h_9 = 0.11294	h_{14} = 0.06020	h_{19} =-0.00727
h_5 = 0.03500	h_{10}=0.13556	h_{15} = 0.03500	

Analytically, the FIR ADB structure can be described by Eq. (2) where the sum over m corresponds to the polyphase commutator with its delay z^{-m} and the sum over i counts the

number of commutators at the input and is responsible for the ADB delays z^{-iM}.

$$H(z) = \sum_{i=0}^{I-1}\left[\sum_{m=0}^{k_i} h_{m+iM}z^{-m}\right]z^{-iM} \qquad (2)$$

Eq. (3) shows the condition for the counting variables of Eq. (2) with $I = \lceil N/M \rceil$[1].

$$k_i = \begin{cases} M-1 & \text{if } i < I-1 \\ R_M(N)-1 & \text{if } i = I-1 \end{cases} \qquad (3)$$

with $N = qM + r$, $0 \le r < |M|$, $r = R_M(N)$ and $q, M, r, N \in \mathbf{Z}$ [2]

2.1. Topology with one input commutator

Applying the concepts described in [10] and using Eq. (2)-Eq. (3) leads to the signal-flow graph shown in Fig. 2 with its appropriate timing.

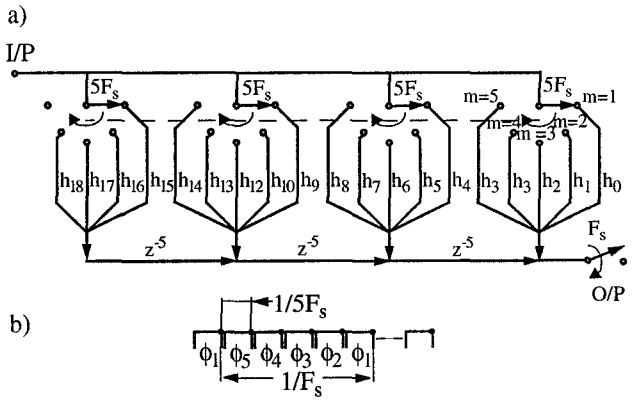

Fig. 2 a) Block-delayed polyphase decimator with 4 input commutators for N=19, M=5, b) timing.

The polyphase filters m_i, $i \in [1, 5]$ are sampled with 4 input commutators. The output of the polyphase filters are then processed through the ADB delay chain to the output of the filter. Since the spread of the decimator coefficients is usually large, the small polyphase coefficients will contribute much more to clockfeedthrough (CLF) errors than the large ones [11], and so, asymmetric errors will result in large distortion of the filter performance. One way of overcoming the CLF error in the polyphase filter at the input branches is to enlarge the gate-source capacitance of the small coefficients. However, this results in a larger die area and longer settling times of the compensated memory cells. Another solution is to multiply the first sum in Eq. (2) into the brackets which means using only one input commutator. The sum of the gate-source capacitance of the m_i^{th} polyphase filter can then be used as an active compensation capacitance. Fig. 3 shows the signal-flow graph of the proposed solution and Eq. (4) gives the corresponding equation.

[1] Following the notation in [15], $\lceil u \rceil$ denotes the smallest integer greater than or equal to u.

[2] Euclid's division theorem for integers.

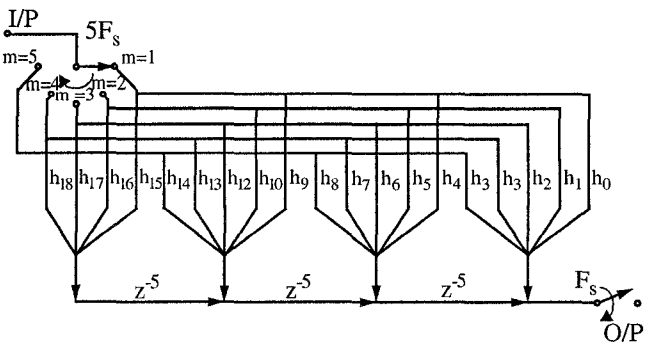

Fig. 3 One input commutator topology for N=19, M=5.

$$H(z) = \sum_{m=0,\,l=0}^{M-1,\,R_M(N)} (h_m z^{-m} + h_{m+M} z^{-m} z^{-M} \ldots \qquad (4)$$

$$+ h_{m+(I-2)M} z^{-m} z^{-(I-2)M} + h_{l+(I-1)M} z^{-l} z^{-(I-1)M})$$

With some scaling of the polyphase coefficients and additional current mirrors the sum of the input capacitances of all polyphase filters can be made equal, such that the injected amount of CLF error behaves, to a first approximation, as an offset. This, in turn, can be compensated for by using differential circuit techniques.

2.2. Linear phase FIR decimator

A FIR filter is considered to be of linear phase if the impulse response satisfies the symmetry conditions $h[N-n] = h[n]$ or $h[N-n] = -h[n]$ for $n = 0,1,...,N$ [12]. For a decimation filter with linear phase, of odd order and for the case of I an even integer[3] Eq. (4) can be rewritten as Eq. (5).

$$H(z) = \sum_{m,l} [h_m (z^{-m} + z^{-l} z^{-(I-c_l)M}) \qquad (5)$$

$$+ h_{m+M}(z^{-m} z^{-M} + z^{-l} z^{-(I-c_l)M})$$

$$+ \ldots + h_{m+(I/2-1)M}(z^{-m} z^{-(I/2-1)M} + z^{-l} z^{-(I-c_l)M})]$$

where the indices m, l are

$$m = \begin{cases} [0, M-1] \text{ if } h_{(.)} < h_{(I/2-1)M} \\ [0, R_M((N-1)/2)] \text{ otherwise.} \end{cases} \qquad (6)$$

$$l = \begin{cases} [R_M(N), 0] \text{ if } h_{(.)} < h_{R_M(N)} \text{ and } c_l = 1. \\ [M-1, 0] \text{ otherwise. If } l = 0 \text{ then } c_l = c_l + 1. \end{cases}$$

When N is even, equations Eq. (5)-Eq. (6) become

$$H(z) = \sum_{m,l} [h_m (z^{-m} + z^{-l} z^{-(I-c_l)M}) \qquad (7)$$

$$+ h_{m+M}(z^{-m} z^{-M} + z^{-l} z^{-(I-c_l)M})$$

$$+ \ldots + h_{m+(I/2-1)M}(z^{-m} z^{-(I/2-1)M} + z^{-l} z^{-(I-c_l)M})]$$

$$+ h_{R_M(N/2)+(I/2-1)M}(z^{-R_M(N/2)} z^{-(I/2-1)M})$$

[3] Similar expressions can be derived for the case of I being odd.

and:

$$m = \begin{cases} [0, M-1] \text{ if } h_{(.)} < h_{(I/2-1)M} \\ [0, R_M(N/2)-1] \text{ otherwise.} \end{cases} \quad (8)$$

$$l = \begin{cases} [R_M(N), 0] \text{ if } h_{(.)} < h_{R_M(N)}, \; c_l = 1. \\ [M-1, 0] \text{ otherwise. If } l = 0 \text{ then } c_l = c_l + 1. \end{cases}$$

For the above cases the number of multiplying coefficients can be essentially halved.

Fig. 4 shows the signal-flow graph of the symmetric multirate FIR filter. Again, to reduce distortion at the input, the one-commutator topology was chosen to enhance the capacitance at the input of each polyphase filter branch.

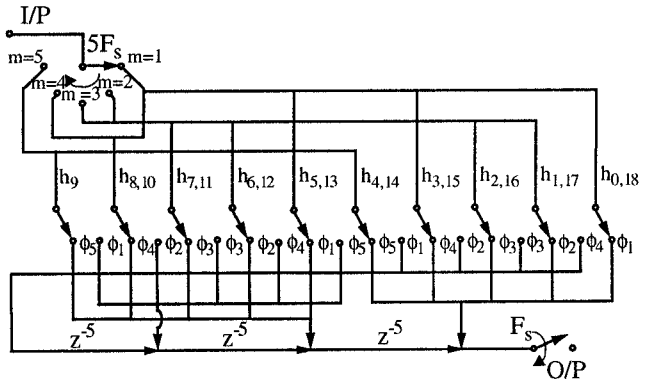

Fig. 4 One input commutator topology for a linear FIR with N=19, M=5.

2.3. One-commutator topology with relaxed timing

To take full advantage of multirate filter design techniques an appropriate clock scheme has to be found to relax the settling specifications of the sample-and-holds at the input. The duty cycle of an individual clock phase can theoretically vary between $1/M$ and 1/2. For the topology under consideration (Fig. 3) duty cycles of 1/2 are possible but only with a complicated ADB-architecture. A good trade off is to use 4/6, e.g. 40% of the clock phase can be used to sample the memories at the input and 60% is for the read-out time before a new sample is taken. Thus, compared to a conventional SI design, a speed-up factor of 4 can be achieved at the input.

Another critical point in FIR design is the maximum signal handling capability of the output summing stage. Since the signal appears as a current, this can easily be fulfilled. Nevertheless, all the partial sums before the output node need to be biased for full signal handling capabilities at their corresponding nodes. A compromise must be made between full parallelism within the ADB blocks at the price of a complicated clock scheme with larger interconnections, and collection of some of the signal paths to the same delay at the penalty of some read-out time reduction. Fig. 5 shows the signal-flow graph of the proposed solution with its appropriate timing, and Fig. 6 the schematic of the circuit. For simplicity, additional current mirrors for the realisation of the negative coefficients and for spread reduction are omitted.

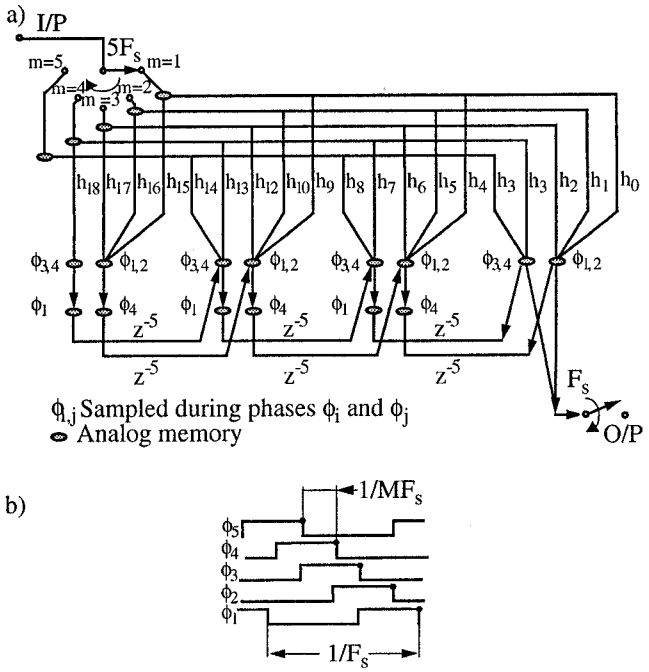

Fig. 5 a) Proposed topology for video decimator with reduced input sampling error and enhanced signal handling capabilities in the ABD-delays b) with relaxed timing.

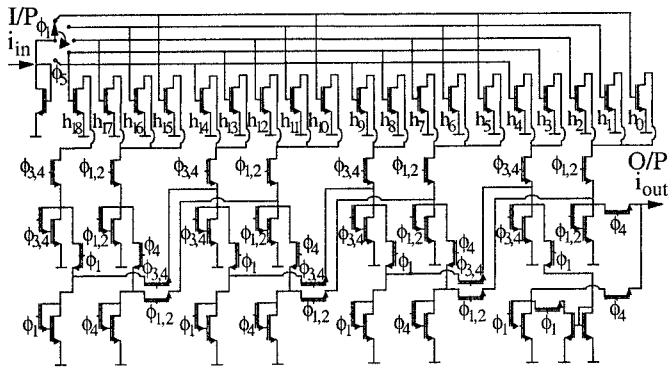

Fig. 6 Circuit of the FIR SI decimator with length N=19, decimating factor M=5 (without current mirrors for the negative coefficients).

The top row shows the filter taps and the input commutator and the second and third row represents the ADB delay chain. The sampled signals are collected in groups of 2 or 3 and later processed separately through the ADB delay line. For example h_{15}, h_{16} and h_{17} are collected during ϕ_1 and ϕ_2 in a 2nd generation SI memory cell and read out during ϕ_4. Thus, during one active delayed block the group is sampled once with a positive sign and once with a negative sign, thereby cancelling CLF to some extent. In the output stage the two groups have to be synchronized to get the output signal at the appropriate clock phase.

III. Electrical Simulation and Results

Fig. 7 shows the amplitude response of the FIR video SI decimator whose input and output sampling frequencies are, re-

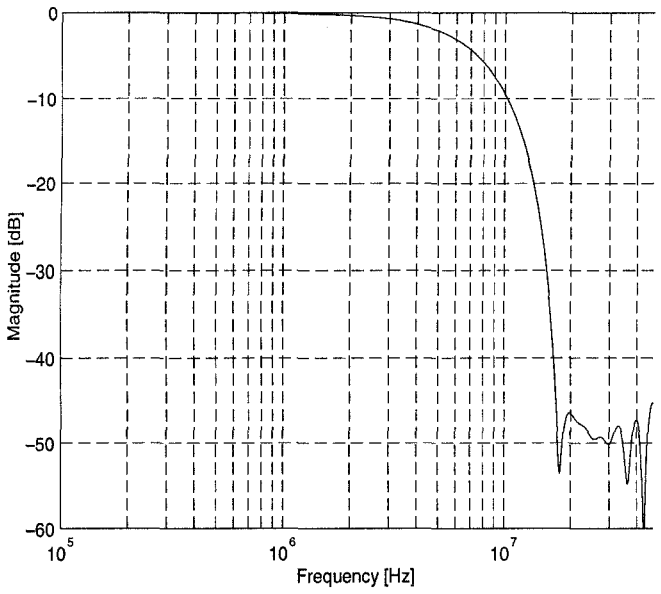

Fig. 7 Electrical simulated amplitude response of the circuit in Fig. 6 using WATSNAP [16] with the coefficients indicated in TABLE 1.

spectively, $5F_s$=135MHz and F_s=27MHz. The circuit is being fabricated using the 0.5µm CMOS process of ATMEL-ES2. The amplitude response is tailored to obtain a cut-off frequency of f_c=6MHz and a minimum rejection of more than 35dB above 16MHz. All memory and source transistors are realized using gain-enhancement-techniques [13] and the ABD memories employ a kind of S^2I-compensation [14].

IV. Conclusions

Switched-current video decimators have been introduced which allow not only the sampling frequency in a subsequent ADC to be reduced by a factor of 5, but also make the design requirements for the continuous time AAF at the input less stringent. The switched-current approach helps to retain full compatibility with CMOS processes, and design methods such as gain-enhancement and S^2I-techniques provide excellent results for an amplitude response tailored to video applications.

V. References

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