Transactions Briefs

Improved Two-Step Clock-Feedthrough Compensation Technique for Switched-Current Circuits

Markus Helfenstein and George S. Moschytz

***Abstract*—A new clock-feedthrough compensation scheme for switched-current circuits is proposed. The scheme is especially suited for the design of delay lines for high-frequency operation. The circuit operates by using an improved two-step technique, in which the input is sampled in a parallel combination of a coarse and a fine memory transistor. Since both transistors are of the same type, large switching transients compared to the conventional S^2I scheme can be avoided. Using the proposed circuit, the coarse memory has considerably more time to settle. Compared to the simple cell, the circuit solution requires only one extra switch and one additional clock phase.**

***Index Terms*— Analog sampled-data circuits, charge injection, sample/hold, switched-current circuits.**

I. Introduction

A major limitation in switched-current applications is clock feedthrough (CFT), which occurs when a switch transistor is connected to a holding capacitor. CFT is caused by carriers released from the channel and from coupling of the clock through the gate-diffusion-overlap capacitances of the switch. Due to the square-law characteristic of the memory MOS transistor, every signal-dependent error voltage on the gate produces both a signal-dependent offset and harmonic distortion of the output current. Besides the well-known dummy switch compensation or the addition of extra gate–source capacitances (physical enlargement or Miller-type techniques [1]), a number of suggestions have been presented to solve the CFT problem. In general, they propose the cancellation of only the signal-dependent part of the CFT [2], [3], both parts [4], or a reduction to some extent, by using, e.g., algorithmic [5], two-step [6], or differential structures [7], [8]. Thus, they basically rely on transistor mismatch, on a repeated sampling of the input current and/or the CFT error itself, or on differential techniques.

In the work presented here, we will describe a modified two-step clock-feedthrough compensation circuit based on an n-memory transistor-only approach. A comparison of experimental data from different compensation circuits, all integrated in a 1-μm CMOS process, will show that the performance of the conventional S^2I scheme [6] can be improved.

The paper first presents a basic review of the CFT problem. This is given in Section II. The modified memory cell is introduced in Section III, and the noise behavior is analyzed in Section IV. Measurement results and a summary are given in Sections V and VI, respectively.

Manuscript received April 29, 1996; revised May 1, 1997. This work was supported by the KWF Jessi-Project, 2302.1 Eureka EU 127. This paper was recommended by Associate Editor W. D. Grover.

The authors are with the Institute of Signal and Information Processing, Swiss Federal Institute of Technology, CH-8092 Zürich, Switzerland (e-mail: helfenst@isi.ee.ethz.ch).

Publisher Item Identifier S 1057-7130(98)02141-7.

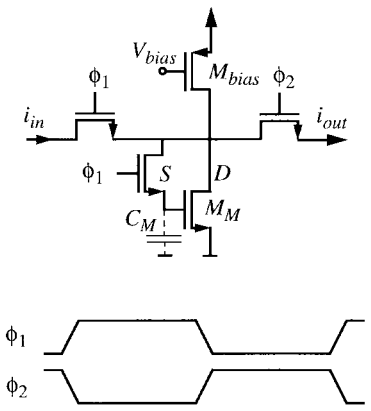

Fig. 1. Second-generation SI memory cell.

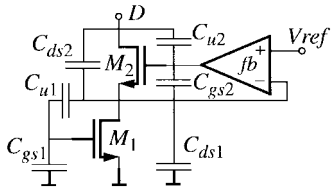

Fig. 2. Gain-enhancement techniques applied to the basic memory cell.

II. CFT Analysis

It is known [8] that the charge injected through the MOS switch S in Fig. 1 introduces an error on the memory capacitance C_M of the memory transistor which can be given as

$$V_{\mathrm{CFT}} = \frac{[\delta(V_H - V_{gs} - V_{TS})L_S C_{\mathrm{ox}} + (V_H - V_L)L_{ovS}C_{\mathrm{ox}}]W_S}{W_M L_M C_{\mathrm{ox}}}. \tag{1}$$

In (1), V_H denotes the high clock amplitude applied to the switch, V_{gs} is the gate–source voltage of the memory transistor $M_M, W_S L_S$ is the area, and V_{TS} the threshold voltage of the switch. A fraction δ of the switch charge flows into C_M, depending on the load at each side of the switch. A second contribution to the CFT error results from the gate–source-overlap capacitance C_{ovS} of the switch.

Another source of CFT error appears in the switch-off state (when ϕ_1 is off) due to transients on the drain of the core transistor (M_M in Fig. 1) via capacitive feedback to C_M. Using the simple small-signal model of the transistor, including C_{gs}, C_{ds}, and C_u for the gate–source, drain–source and Miller capacitance, respectively (Fig. 2), it can be shown that a step ΔV applied at the drain of the core transistor introduces an error voltage at the gate of the corresponding transistor which can be expressed as

$$\Delta V_{gs} = \Delta V C_u/(C_u + C_{gs}). \tag{2}$$

Using a local feedback network (Fig. 2) to stabilize the drain–source voltage of the main transistor M_1 is a well-known technique to improve the gain of a single transistor $g_{m2}g_{ds2}$ by the intrinsic

gain of the cascode transistor and the additional gain fb of the feedbackloop [9]. The output resistance of a cascoded transistor can then be calculated as

$$r_{\rm out} = r_2 + r_1[1 + g_{m2}r_2(1 + fb)] \tag{3}$$

where r_i is the small-signal output resistance and g_{mi} is the transconductance of transistor M_i $(i = 1, 2)$. As a side effect of this gain-enhancement technique, not only is the input-to-output conductance ratio significantly improved, but also the Miller capacitance of the core transistor can be reduced by the factor $g_{m1}/(g_{m2}f_b)$. This lowers the error introduced through C_u and the apparent capacitance seen at the gate of M_1 significantly, especially for cases with large feedback factors. Using (3), it can be shown that the drain–source capacitances of M_1 and M_2 are reduced by the factor $g_{ds2}/(g_{m1}f_b)$ and $g_{ds1}/(g_{m2}f_b)$, respectively, which further reduces capacitive coupling. Although, as shown, a reduction of the capacitive feedthrough error from (2), is possible, a good design should, in terms of speed, keep the transients between the memory and the bias transistor as small as possible.

III. Improved Two-Step Compensation Circuit

The basic S^2I cell was invented by Hughes *et al.* as a two-step method of compensating for clock feedthrough in switched-current circuits [6]. It uses not only the primary memory transistor (M_M in Fig. 1), but also the current source transistor $M_{\rm bias}$ such that the biasing transistor acts as a current source in a first step, and as an error compensation in a second step. Since the scheme needs to switch between the n- and p-channel memory, transients occurring at the drains of the appropriate transistors are difficult to handle, even with the gain-enhancement techniques mentioned above. Several attempts at multistep CFT cancellation using only n- or p-type transistors as memories have been reported. They range from algorithmic memory cells, which use two auxiliary cells and a six-phase clocking scheme [5] for operation in a CFT-measure and input-sample mode, to the S^nI cell [10], which proposes an n-fold sampling of the CFT error, and uses $2n$ additional clock phases. These methods lead to clock complexity, and to a large sampling time reduction in the coarse memory. In addition, large transients on the drain side of the memory cell may be involved when switching from the n- to the p-memory cell. This results in errors as given in (2).

In what follows, we present an improved two-step clock-feedthrough compensation for switched-current circuits. This approach in large part compensates the error given in (1), and considerably reduces ΔV in (2).

The proposed circuit is shown in Fig. 3. The basic idea is to split the memory transistor into a coarse and a fine memory using only n-channel transistors, and to use an additional input sampling phase ϕ_{1c}. The sample-and-hold (S/H) cell consists of a current source formed by $M_{\rm bias}$, a coarse and a fine memory transistor M_{Mc} and M_{Mf}, respectively, and the two switches S_c and S_f. The switches have to be properly designed to assure that their corresponding memory transistors have time to settle [8]; thus, the switch area of the coarse transistor is larger than that of S_f. The operation is as follows. During phase ϕ_{1c}, the input current $i_{\rm in}$ is sampled into the coarse and fine memory cells. During phase ϕ_{1c}, the drain–source currents I_c and I_f are given by

$$I_c = (J + i_{\rm in})\frac{g_{mc}}{g_{mc} + g_{mf}} \tag{4}$$

and

$$I_f = (J + i_{\rm in})\frac{g_{mf}}{g_{mc} + g_{mf}} \tag{5}$$

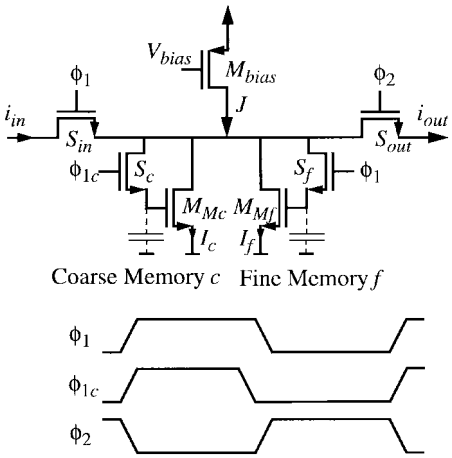

Fig. 3. Improved S^2I circuit with clock diagram.

where J is the bias current flowing through $M_{\rm bias}$ and g_{mi} is the transconductance of the transistor $i, i \in [f, c]$. The coarse memorizing is now completed, and after opening S_c, a signal-dependent error current δi, resulting from charge injection of the switch, is added to the drain–source current of I_c. Thus,

$$I_c = (J + i_{\rm in})\frac{g_{mc}}{g_{mc} + g_{mf}} + \delta i. \tag{6}$$

Since δi is small and the drain holds its voltage value, *only a small transient occurs after* ϕ_{1c}. During the remaining time period ϕ_1,[1] the coarse memory operates as a current sink, demanding the current previously sampled, i.e., (6), and the fine memory, still diode connected, delivers current as required to fulfill Kirchhoff's current law at the summing node. Because the input current is still being sampled, the only current change in the fine memory will be the CFT part introduced by the coarse memory. Thus, I_f is given by

$$I_f = (J + i_{\rm in})\frac{g_{mcf}}{g_{mc} + g_{mf}} - \delta i. \tag{7}$$

During phase ϕ_2, switch S_f is open, and a small error Δi is introduced into the fine memory, again due to charge injection. Since the switch area of the fine memory is close to the minimum transistor size, this secondary error current $\Delta i \ll \delta i$, and the injection error is considerably reduced. To give a rough estimate of the error reduction thereby obtained, the CFT current $i_{\rm CFT}$ can be approximated by $i_{\rm CFT} = g_m V_{\rm CFT}$, where $V_{\rm CFT}$ is given by (1). To a first order, the CFT error voltage of the memory transistor is proportional to the ratio of the switch and the corresponding memory transistor area [11], so that the error current introduced by CFT is approximately reduced by the ratio of the coarse to the fine memory transconductances. Especially in high-frequency designs where, on the one hand, to achieve the desired speed a large transconductance is needed, and on the other hand, good settling behavior demands large switches, this factor can easily be more than ten. Additional capacitance connected to the gate of the fine transistor results in a larger reduction using only small areas. The resulting error current Δ_i may be viewed as signal dependent, but the dependency is reduced by the same amount as the overall error. It can be shown that by choosing the appropriate transistor ratio, a tradeoff between a small, signal-dependent error versus an offset is imposed. This circuit can be combined with dummy switch compensation techniques or even the S^nI approach. Since the time to settle for the coarse memory is now longer than that of the

[1] In a practical design, the switch-on time of the current steering transistor $S_{\rm in}$ is slightly longer than the switch-on time of the voltage sampling transistor S_f. Nevertheless, in what follows, we will not distinguish between the two.

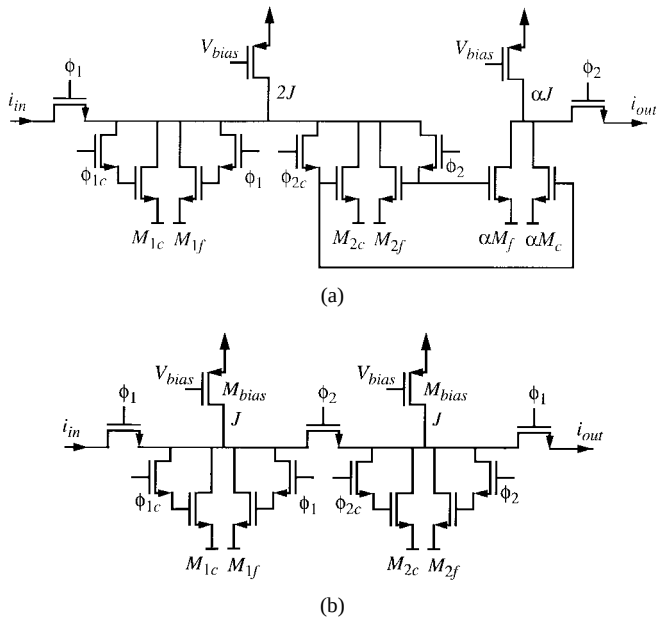

Fig. 4. (a) Noninverting lossless SI integrator and (b) SI delay chain using the modified two-step approach.

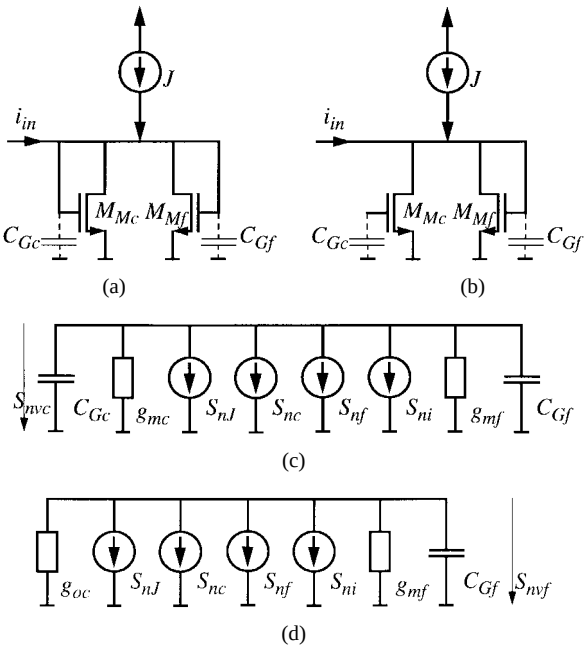

Fig. 5. Memory cell in (a) the sampling phase ϕ_{1c}, in (b) the sampling phase ϕ_1, and the corresponding noise-equivalent circuit for the phases (c) ϕ_{1c} and (d) ϕ_1. The S_n correspond to the power spectral densities of the bias source S_{nJ}, the coarse and fine memory transistors S_{nc} and S_{nf}, and the input signal S_{ni}, respectively.

original circuit, a reduction in the transistor power consumption or the area can also be achieved, while improving its transient behavior. Additional reduction of the CFT error can be achieved when using extra compensation capacitances at the gate of the fine memory cell. As in the case for the basic cell, this similarly reduces the sampling rate of the circuit.

Using this memory cell in a simple second-generation integrator configuration, the initial spread of the circuit will be enlarged. Fig. 4(a) shows the noninverting lossless integrator including an output scaling stage with factor α. Thus, the spread will be the ratio between the coarse and the fine memory transistor areas divided by α. There is no spread enlargement if the two-step approach is applied to the design of delay lines as in Fig. 4(b). This makes it ideally suitable for the design of active-delayed blocks [12] in FIR decimator structures [13].

In the following section, the noise behavior of the modified two-step memory cell is investigated.

IV. Noise Analysis of the Two-Step SI Memory Cell

The noise analysis of switched-current memory cells can be found in [8, Chs. 4 and 5] and [1]. In this section, these analysis methods are applied to the modified two-step SI memory cell following the notation in [1].

In switched-current circuits, we must distinguish between thermal and $1/f$ noise. The power spectral density function (PSD) is a common term used in the noise analysis of circuits. It expresses the ratio of the mean-squared noise current to the frequency interval. The PSD functions of the thermal and $1/f$ noise, S_t and S_f, are well known for MOS transistors. They are given in the literature as $S_t = 8/3 \cdot (kTg_m)$ and $S_{1/f} = (K_n f g_m^2)/(C_{\rm ox} W L |f|)$, respectively, where k is Bolzmann's constant, T is the absolute temperature, g_m is the transconductance of the transistor with width W and length L, K_{nf} is the flicker noise coefficient, and $C_{\rm ox}$ is the gate capacitance per unit area.

To take into account the influence of continuous-time noise to sampled current noise, we calculate the PSD of the noise voltage across the gate capacitor of the memory transistor to obtain the equivalent stored noise current. From the noise-equivalent circuit for phase ϕ_{1c} shown in Fig. 5(a) and (c), we get the PSD of the voltage noise process across the gate capacitor of the coarse transistor as

$$S_{nv_c} = \frac{S_{nJ}(\omega) + S_{nc}(\omega) + S_{nf}(\omega) + S_{ni}(\omega)}{(g_{mc} + g_{mf})^2 + \omega^2 (C_{Gc} + C_{Gf})^2} \tag{8}$$

where the $S_n(\omega)$ correspond to the power spectral densities of the bias source S_J, the coarse and fine memory transistors S_{nc} and S_{nf}, and the input signal S_{ni}, respectively. It has been shown that in the basic SI memory cell, low-frequency noise is effectively removed due to the correlated double sampling process [8, Ch. 4]. The same holds for the modified SI memory cell. The variance σ_{ic}^2 of the stored noise current in the coarse memory M_{Mc} can be computed as

$$\sigma_{ic}^2 = \frac{g_{mc}^2}{2\pi} \int_0^\infty S_{nv_c}(\omega)\, d\omega = \frac{g_{mc}^2}{4(g_{mc} + g_{mf})(C_{Gc} + C_{Gf})} (S_{nJ} + S_{nc} + S_{nf} + S_{ni}) \tag{9}$$

where all of the PSD's in (9) are assumed to be constant white noise. After switching off ϕ_{1c}, the only remaining sampling transistor is M_{Mf}, and the corresponding noise-equivalent circuit is given in Fig. 5(b) and (d). The noise current previously stored in the coarse memory σ_{ic} is now sampled as an offset current in the fine memory. Assuming $g_{oc} \ll g_{mf}$, the noise contribution of the output impedance of transistor M_{Mc} can be neglected. Thus, the corresponding PSD process over the gate–source capacitance C_{Gf} of the fine memory can be given as

$$S_{nv_f} = \frac{S_{nJ} + S_{nc} + S_{nf} + S_{ni}}{g_{mf}^2 + \omega^2 C_{Gf}^2}. \tag{10}$$

This can be integrated to obtain the variance σ_{if}^2 of the stored noise current in the fine memory M_{Mf} as

$$\sigma_{if}^2 = \frac{g_{mf}}{4C_{Gf}} (S_{nJ} + S_{nc} + S_{nf} + S_{ni}). \tag{11}$$

Finally, the stored noise currents and the noise offset introduced by the coarse transistor sum up at the drain of the transistors, resulting

in the variance σ^2_{itot} of the noise current at the output of the sample-and-hold, where $\sigma^2_{itot} = \sigma^2_{if}$:

$$\sigma^2_{itot} = \left(\frac{g_{mf}}{4C_{Gf}}\right)\left[\frac{8}{3}kT(g_{mJ} + g_{mtot}) + S_{ni}\right]. \qquad (12)$$

If R is the ratio of the widths of the sum of the coarse and fine to the fine memory transistors, i.e., $R = (W_c + W_f)/W_f$, the ratios of the transconductances and the gate–source capacitances can also be expressed as R, i.e., R is equal to $I_{tot}/I_f, C_{Gtot}/C_{Gf}$, and g_{mtot}/g_{mf}. Thus, (12) simplifies to

$$\sigma^2_{itot} = \frac{2kTg^2_{mtot}}{3C_{Gtot}}\left(1 + \frac{g_{mJ}}{g_{mtot}}\right) + \frac{g_{mtot}}{4C_{Gtot}}S_{ni} \qquad (13)$$

which is equivalent to the result proposed by Guggenbühl *et al*. [1]. Not surprisingly, since the fine memory transistor operates not only at a lower current level, but also with lower gate–source capacitance, and since the noise contribution of the coarse memory is treated as an offset, the total noise current at the output is similar to the noise current of the simple memory cell with equal transconductance value.[2] For the circuit proposed by Hughes *et al*. [6], (13) holds for $g_{mtot} = g_{mJ}$ and $C_{Gtot} = C_{GJ}$, where C_{GJ} is the gate–source capacitance of the bias transistor M_{bias}. If this is not the case, then g_{mtot} has to be replaced by g_{mJ}, and vice versa, g_{mJ} by g_{mtot}. Likewise, exchange C_{Gtot} and C_{GJ}.

V. Measurement Results

We have implemented and tested various clock-feedthrough compensation circuits using the 1-μm SACMOS process [14]. For comparison purposes, a memory cell without CFT reduction techniques, the original S^2I circuit, the modified S^2I, and the compensation scheme proposed in [4, set (d)] have been considered. The circuits are denoted as *SI_simple*, *S2I_orig*, *S2I_mod*, and *SI_match*, respectively. To improve accuracy, regulated cascode current sources and current mirrors were used (RGC [15]). The bias current J was chosen to be 100 μA, and the circuit was operated at a 3-V supply. On-chip measurements of very small currents in the megahertz range with good resolution are difficult to carry out without relying on transistor matching. Therefore, the ratio of the rms value of the signal to the rms sum of all other spectral components within the measurement bandwidth, including distortion components, i.e., THD + N, has been chosen as a factor of merit. For a memory transistor with $W_M/L_M = 150\,\mu\text{m}/10\,\mu\text{m}$ and a clock frequency of 1 MHz ($t_{rise} = t_{fall} = 1$ ns), THD + N was measured for input currents between 20 and 80 μA at an input frequency of 10 kHz. Neglecting the input noise contribution in (13), the standard deviation of the stored noise current of the circuits *SI_simple*, *S2I_orig*, and *S2I_mod* can be calculated with $g_{mtot} = 0.6$ mV/A, $g_{mtot} = g_{mJ}$, and $C_{gstot} = 2.5$ pF as $\sigma_{iout} \approx 27$ nA.[3]

For the circuit *SI_match*, the noise level is a factor of $\sqrt{2}$ lower than that of the others because the memory transistor is of the same size as that of *SI_simple*, and the additional compensation network contributes to the capacitance seen at the gate of the memory.

The output spectrum of *S2I_mod* was measured for a coarse and a fine cell of $W_c/L_c = 100\,\mu\text{m}/10\,\mu\text{m}$ and $W_f/L_f = 50\,\mu\text{m}/10\,\mu\text{m}$, respectively, with a small additional capacitance at the gate of the fine memory. The switches used to make the diode connections around the appropriate transistors were chosen to be $2\,\mu\text{m}/1\,\mu\text{m}$ and $1\,\mu\text{m}/1\,\mu\text{m}$. At a clock frequency of 1 MHz, the sampling time was 42% for the coarse memory and 49% for the fine memory. Thus, the sampling interval for the main memory was enlarged considerably compared to that of the originally proposed cell. Fig. 6 shows the output spectrum of a simple sample-and-hold cell for the *S2I_mod* circuit for 60% modulation. The second harmonic is 62.5 dB below the fundamental, and the third is more than 72 dB below. A doubling of the sampling frequency increases the distortion by about 2.5 dB. The measurements were performed using a HP3588 spectrum analyzer.

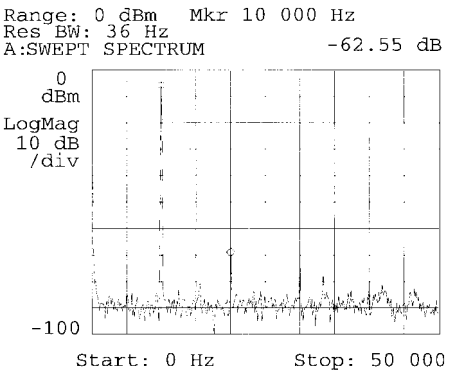

Fig. 6. Output spectrum of circuit S^2I_{mod} for 60% modulation, 10-kHz input frequency, 1-MHz clock frequency, and 3-V power supply.

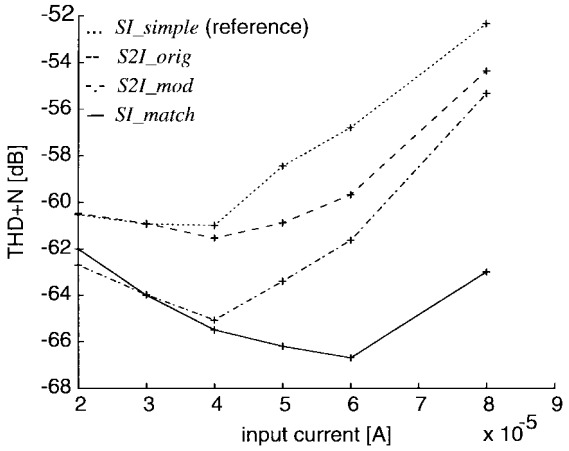

Fig. 7. THD + N versus the input current for different sample-and-holds. The measurements were taken for the circuits *SI_simple* ($\cdots$), *S2I_orig* (--), *S2I_mod* (-·-), and *SI_match* (__), an input sampling frequency of 10 kHz, and a clock frequency of 1 MHz.

Our measurement results are summarized for the different circuits in Fig. 7, where the dependencies of the THD + N on the input signal current are shown. All measurement values are mean values for a sample of five chips, proving that the behavior is robust with respect to parameter variations. An HP 3561A dynamic signal analyzer was used to calculate THD + N over an average of ten measurements per sample and a signal bandwidth of 100 kHz. As can be seen, depending on the input current, *S2I_mod* is between 1 and 3.5 dB better than *S2I_orig*. Compared to *S2I_simple*, the improvement is in the range of 4 dB. *SI_match* achieves the lowest distortion values, although these measured results are worse than expected (see [4]) due to a transistor mismatch which is larger than the values reported in [16], [17]. Note, however, that with regard to power and area efficiency, the multiphase circuit introduced here is more than three times better than the one based on matching. Of course, in a differential structure, part of the circuit *SI_match* can be shared (for example, the offset term in [4] need not be cancelled), and so, power and area are reduced. The results are summarized in Table I. A comparison of the maximum sampling capabilities of the different compensation techniques with

[2] Further, as in [8, Chs. 4 and 5], one can distinguish between direct and sampled noise.

[3] In this example, having a bandwidth of 60 MHz, the direct noise makes a contribution to the total noise power of 12 nA.

TABLE I
MEASURED SAMPLE-AND-HOLD PERFORMANCE FOR DIFFERENT CIRCUITS

Sample-and-Hold circuits	*SI_simple*	*S2I_orig*	*S2I_mod*	*SI_match*
THD @ 50% modulation, f_{in}=10kHz, worst case values of a sample of 5.	57 dB	59 dB	62 dB	64 dB
Power supply	3 V	3 V	3 V	3 V
Power (for Vdd = 3 V) (incl. regulated cascodes, excl. bias generation network)	0.35 mW	0.35 mW	0.35 mW	0.86 mW
Active area (incl. regulated cascodes, switches, wires, excl. bias generation network)	0.023 mm^2	0.025 mm^2	0.025 mm^2	0.070 mm^2
Relative max. sampling rate compared to simple S/H. (ε denotes to the time M_{Mf} needs to resample δi.)	1	1/2	1/(1+ε)	1/2.33

the basic sample-and-hold, i.e., the total capacitance to be driven during the sampling phases to the gate–source capacitance of a single memory transistor, leads to the last line in Table I. As can be seen, speed performance is best for the simple and the proposed circuit, whereas the one based on matching suffers due to the additional compensation stage. As simulations of the circuit proposed in [13] show, the accuracy of SI_mod could be increased by enlarging R, i.e., $R = (W_c + W_f)/W_f$.

VI. SUMMARY

It has been shown that by using only n-channel transistors in a two-step switched-current memory cell, the performance of the basic sample-and-hold can be improved. Compared to the original proposal, the settling time of the main memory was increased by about 30%; consequently, to achieve the same precision, power and area can be reduced. For a typical design, the noise behavior of this modified two-step approach is similar to the basic sample-and-hold.

We have integrated and tested several sample-and-hold structures in a 1-μm CMOS process, and have reported on the differences with respect to power, area, and THD versus the input current. For the modified two-step approach, a THD of -62 dB (worst case) for 50% modulation, at an input sampling frequency of 10 kHz and a clock frequency of 1 MHz, was measured. For a power supply of 3 V, the power consumption was measured to be 350 μW.

Experimental results applying the proposed solution in a switched-current active-block-delay line are in preparation [13].

ACKNOWLEDGMENT

The authors would like to acknowledge the anonymous reviewers for their useful comments and suggestions.

REFERENCES

[1] W. Guggenbühl, J. Di, and J Goette, "Switched-current memory circuits for high-precision applications," *IEEE J. Solid-State Circuits*, vol. 29, pp. 1108–1116, Sept. 1994.
[2] T. S. Fiez, D. J. Allstot, G. Liang, and P. Lao, "Signal-dependent clock-feedthrough cancellation in switched-current circuits," in *Int. Conf. Circuits Syst.*, Shenzhen, China, 1991, pp. 785–788.
[3] M. Song, Y. Lee, and W. Kim, "A clock feedthrough reduction circuit for switched current systems," *IEEE J. Solid-State Circuits*, vol. 28, pp. 133–137, Feb. 1993.
[4] M. Helfenstein and G. S. Moschytz, "Clock-feedthrough compensation technique for switched-current circuits," *IEEE Trans. Circuits Syst.*, vol. 42, pp. 229–231, Mar. 1995.
[5] C. Toumazou, N. C. Battersby, and C. Maglaras, "High-performance algorithmic switched-current memory cell," *Electron. Lett.*, vol. 26, pp. 1593–1595, Sept. 1990.
[6] J. Hughes and K. Moulding, "A two-step approach to switched-currents," in *Proc. IEEE Int. Symp. Circuits Syst. ISCAS93*, Chicago, IL, 1993, pp. 1235–1238.
[7] Y. Sugimoto, "A 1.6V 10-bit 20MHz current-mode sample and hold circuit," in *Proc. IEEE Int. Symp. Circuits Syst. ISCAS95*, Seattle, WA, 1995, pp. 1332–1335.
[8] C. Toumazou, J. B. Hughes, and N. C. Battersby, *Switched-Currents, An Analogue Technique for Digital Technology*. London, U.K.: Peter Peregrinus, Ltd., 1993.
[9] K. Bult and G. J. Geelen, "A fast-settling CMOS opamp for SC circuits with 90-dB DC gain," *IEEE J. Solid-State Circuits*, vol. 25, pp. 1379–1384, Dec. 1990.
[10] C. Toumazou and S. Xiao "An N-step charge injection cancellation scheme for switched current circuits," *Electron. Lett.*, vol. 30, pp. 680–681, Apr. 1994.
[11] S. J. Daubert, D. Vallancourt, and Y. P. Tsividis, "Current copier cells," *Electron. Lett.*, vol. 24, pp. 1560–1562, Dec. 1990.
[12] J. E. Franca and S. Santos, "FIR switched-capacitor decimators with active-delayed block polyphase structures," *IEEE Trans. Circuits Syst.*, vol. 35, pp. 1033–1037, Aug. 1988.
[13] M. Helfenstein, J. E. Franca, and G. S. Moschytz, "Design techniques for HDTV switched-current decimators," in *Proc. IEEE Int. Symp. Circuits Syst. ISCAS96*, Atlanta, GA, 1996, pp. 195–198.
[14] R. E. Luescher and J. Solo de Zaldivar, "A high density CMOS process," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, 1985, pp. 260–261.
[15] E. Säckinger and W. Guggenbühl, "A high-swing, high-impedance MOS cascode circuit," *IEEE J. Solid-State Circuits*, vol. 25, pp. 289–298, Feb. 1990.
[16] K. R. Lakshmikumar, R. A. Hadaway, and M. A. Copeland, "Characterization and modeling of mismatch in MOS transistors for precision analog design," *IEEE J. Solid-State Circuits*, vol. SC-21, pp. 1057–1066, Dec. 1986.
[17] M. J. Pelgrom, A. C. Duinmaijer, and A. P. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, pp. 1433–1440, Oct. 1989.