High-level Comparison of Control-Bounded A/D Converters and Continuous-Time Sigma-Delta Modulators

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***Abstract*—In this paper, behavioural circuit simulations are used to compare the leapfrog control-bounded analog-to-digital converter to relevant continuous-time sigma-delta modulators in terms of nominal performance and sensitivity to component variations, clock jitter and finite gain-bandwidth product. Simulations show that the nominal performance of the leapfrog is similar to that of a continuous-time sigma-delta modulator of the same loop filter order and with the same number of quantization levels. Component variations in the leapfrog's analog system will introduce errors in the final output, unless the coefficients of the reconstruction filter are modified accordingly. Nevertheless, the simple, modular structure, analytical stability guarantee and single-bit quantizers make the leapfrog an interesting alternative to conventional continuous-time sigma-delta modulators.**

***Index Terms*—Control-Bounded Analog-to-Digital Conversion, Continuous-time sigma-delta, ADC, Component Variations, jitter, gain-bandwidth**

I. Introduction

Control-bounded analog-to-digital conversion was proposed in [1] and further developed in [2] and [3]. The conversion principle builds on the idea that analog amplification, counteracted by a digital control, amounts to an implicit A/D conversion. This general idea enables a flexible design framework that promotes novel co-optimization between the analog and digital domain of an analog-to-digital converter (ADC) [2], [3]. Previously, a solid mathematical foundation was presented together with a number of fundamental ADC design proposals. These designs were mainly verified through behavioural simulations and discrete component prototypes. However, no transistor level implementation on silicon has been reported so far.

Two of the fundamental architectures introduced in [2] are the so called chain-of-integrators (CI) and leapfrog (LF) ADC, see Fig. 1. These architectures consist of a chain of integrators, with or without leapfrog feedback, where each integrator is individually stabilized by local digital control. The simple, modular structure, analytical stability guarantee and single-bit quantizers makes these structures attractive from an implementation point of view.

Although conceptually different, these architectures structurally resembles those of a continuous-time sigma-delta modulator (CTSDM). It is therefore interesting to compare the nominal performance of a CI and LF ADC to CTSDMs with the same oversampling ratio (OSR) and loop filter order. Additionally, it is reasonable to assume that the main performance limitations associated with CTSDMs will also apply to control-bounded analog-to-digital converters (CBADCs).

In this paper, we compare the CI and LF ADC to comparable CTSDMs in terms of nominal performance and sensitivity to component variations, clock jitter and finite gain-bandwidth product (GBWP) of the amplifiers.

The paper is organized as follows. The CI and LF ADCs are presented in Section II together with a brief introduction to the control-bounded conversion concept. The nominal performance comparison to CTSDMs is presented in Section III before sensitivity to component variations, clock jitter and finite GBWP is addressed in Sections IV to VI. Finally, conclusions are drawn in Section VII.

II. The Leapfrog CBADC

A homogeneous, N-th order, LF analog system is defined by a system of differential equations of the form

$$\dot{x}_\ell(t) = \beta x_{\ell-1}(t) + \alpha x_{\ell+1}(t) + \kappa s_\ell(t) \tag{1}$$

for $\ell \in [1, \ldots, N]$ where $x_0(t) \triangleq u(t)$ refers to the input signal, and $x_{N+1}(t) \triangleq 0$. Such a LF analog system, together with a local digital control, operated with a control period $1/f_s$, is shown in Fig. 1. The CI analog system is a special case of the LF analog system were $\alpha = 0$.

The basic principle of the CI and LF structures is to amplify the input signal through a chain of integrators. The output of each integrator is interpreted as a state of the analog system and each state is being stabilized by the non-return-to-zero (NRZ), single-bit control signals $s_1(t) \ldots s_N(t)$.

The final ADC output is obtained by running the control signals $s_\ell(t)$ through the finite impulse response (FIR) filter

$$\hat{u}[k] = \sum_{j=-K_1}^{K_2-1} \sum_{\ell=1}^{N} h_{j,\ell} \cdot s_\ell(t_{k+j}), \tag{2}$$

referred to as the reconstruction filter. The filter coefficients $h_{j,\ell}$ are calculated based on a parameterized description of the analog system (see (1)), and the reader is referred to [3] for a complete derivation.

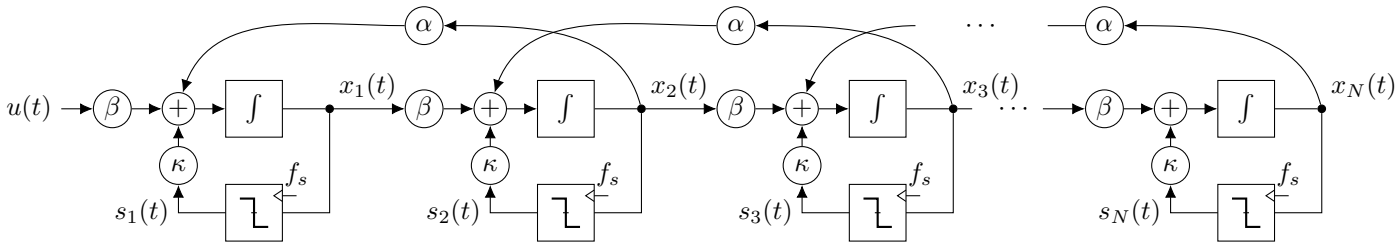

Fig. 1: A N-th order homogeneous chain-of-integrators (CI) ($\alpha = 0$) and leapfrog (LF) ($\alpha < 0$) control-bounded ADC.

As shown in [2], the performance of a LF CBADC may be expressed in terms of $G(\omega)$, which denotes the transfer function from $u(t)$ to $x_N(t)$. For a bandwidth frequency $\omega_{\mathcal{B}}$, the signal-to-noise ratio (SNR) of the ADC output may be approximated as

$$\text{SNR} \propto \left(P_{x_N} \int_0^{\omega_{\mathcal{B}}} |G(\omega)|^{-2} d\omega \right)^{-1}, \tag{3}$$

where P_{x_N} is the total power of $x_N(t)$. The SNR of a CBADC is therefore improved by increasing the in-band amplification of the analog system or reducing the magnitude of $x_N(t)$.

A. Parametrization

Parametrizing the LF ADC for a target specification involves choosing the parameters β, α, κ and f_s such that the ADC achieves a target SNR over a desired bandwidth $\omega_{\mathcal{B}}$. Due to the chain-like structure of the CI and LF analog system, it follows from (3) that SNR $\propto \beta^{2N}$. By a recursive argument [3], it may be shown that the analog system has guaranteed stability if

$$f_s = 2|\beta| \text{ and } \kappa = -\beta. \tag{4}$$

In other words, increasing the SNR by increasing β comes at a cost of higher control frequency, f_s.

In contrast to the CI, the LF can have complex poles in the transfer function, because of the feedback paths in the analog system. As a result, the analog system can provide a certain amplification over a wider bandwidth for the same β. According to (3), the LF will therefore achieve a higher SNR for the same f_s, compared to the CI.

III. Nominal Performance Comparison

In this section, we compare the nominal performance of the CI and LF CBADC against various CTSDMs for different orders N. In the following simulations, the LF is parameterized for a target SNR of 90dB (cf. [2]), where β and f_s satisfy the analytical stability guarantee of (4). The CI is parameterized with the same OSR and for both the CI and LF we use a full scale (FS) input amplitude. The simulations are performed using the circuit simulator Spectre, where the comparators and active-RC integrators are modelled using verilog-a and the input signal is a sinusoidal with frequency $f_i = f_s/1024$.

The number of coefficients K_1 + K_2 used for the reconstruction filter (2) must be sufficiently large, such that it does not limit the SNR. For simplicity K_1 = K_2 = 2^{10} was used in all simulations in this paper, which is a number that is intentionally chosen larger than necessary for the target SNR of 90dB.

The CTSDMs are synthesized using the Schreier MATLAB Toolbox [4] with optimized placement of the noise transfer function (NTF) zeros. For each modulator, the OSR is chosen the same as for the LF, and the maximum out-of-band NTF gain, $||\text{NTF}||_\infty$, is empirically maximized by verifying stability with a 0.5FS sinusoidal and DC input. Both the CBADCs and CTSDMs are simulated with an NRZ feedback digital-to-analog converter (DAC).

The simulation results are shown in Fig. 2. For each N, CTSDMs with an Nth order loop-filter are simulated with an N level (SD NL), 1 bit (SD 1B) and N bit (SD NB) quantizer. For each N, both cascade of resonators with feedback (CRFB) and cascade of resonators with feedforward (CRFF) structures are simulated and the one with highest SNR is shown in the plot. The choice of quantization levels is motivated by the following observations. As the CI and LF ADCs has N output bits per clock period, a CTSDM with an N bit quantizer would have the same output bitrate. However, the required hardware complexity will be higher for an N bit quantizer compared to N single bit quantizers. To match the number of quantization levels, CTSDMs with N level quantizers are simulated for N equal 2, 4 and 8.

The figure shows that the LF ADC has a similar nominal performance as a CTSDM with an N level quantizer. In other words, if the N level quantizer of an Nth order CTSDM is implemented as a flash ADC, a similar nominal performance could be achieved by using the same comparators as local control on a LF analog system, thereby avoiding the linearity issues associated with the multi-level feedback DACs.

Furthermore, Fig. 2 show that the SNR of the LF ADC increase by approximately 12dB per N relative to an Nth order, single-bit CTSDM. As expected, the CTSDMs with N bit quantizers has an nominal SNR advantage. It should be noted that, in these comparisons, the CI and LF ADC has an analytical stability guarantee, while the $||\text{NTF}||_\infty$ of the CTSDMs is empirically optimized for the given quantizer

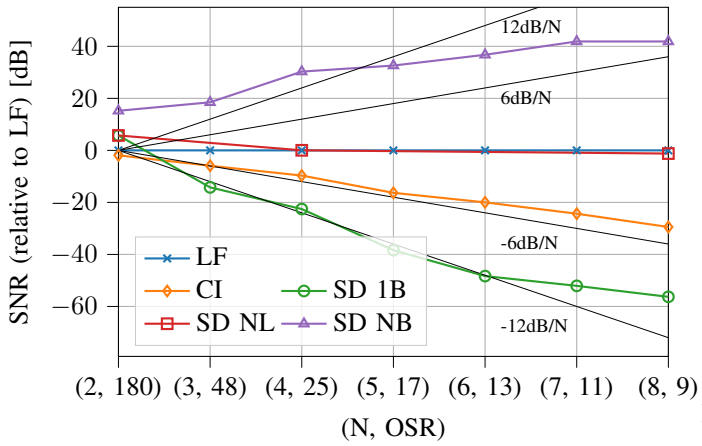

Fig. 2: Simulated and normalized SNR for a LF and CI CBADC compared against CTSDMs with single bit (1B), N-level (NL) and N-bit (NB) quantizers.

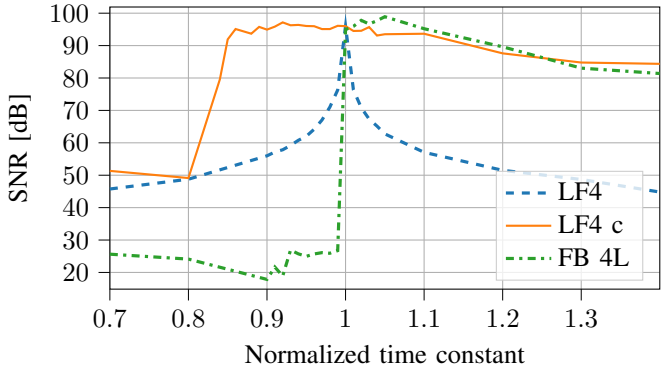

Fig. 3: Simulated SNR vs. normalized time constant for a 4th order CRFB CTSDM with a 4 level (FB 4L) quantizer, and a 4th order LF ADC with (LF4 c) and without (LF4) corrected filter coefficients.

and OSR. Higher SNR could therefore be achieved for the CBADCs, at the expense of reduced stability margin, by violating the stability guarantee of (4).

Finally, we note that the SNR of the CI decrease with approximately 6 dB per N relative to the LF. This is explained by the extended bandwidth of the LF analog system, as briefly discussed in Section II-A.

IV. Component Variations

For CTSDMs implemented with active-RC integrators, the time-constants are subject to significant process variations due to the inaccuracy of the RC-product. When the time-constants are increased from their nominal value, the loop-filter become less aggressive, resulting in weaker quantization noise suppression and reduced nominal performance. On the other hand, lower time-constants increase the nominal performance, but also the risk of instability [5]. As the SNR of a CBADC is proportional to the in-band amplification of the analog system (see (3)), a similar behaviour should be expected for the LF ADC.

Fig. 3 shows simulated SNR versus normalized time constant values for the 4th order LF ADC, and the 4 level (4L) CRFB CTSDM from Fig. 2. In the simulations, all time constants are varied by the same amount, which may be considered the worst-case scenario in terms of stability [6].

As the reconstruction filter of a CBADC is derived from a parameterized description of the analog system, we would expect a reduced SNR if the integrator time constants change without the reconstruction filter being modified accordingly. From Fig. 3 we see that this is indeed the case, where the orange and blue lines shows the SNR of the LF with and without corrected filter coefficients, respectively. For this particular system, the SNR reduction due to mismatch in the filter coefficients is more than 20dB for a 5% variation in time constants.

When the reconstruction filter is corrected to match the analog system, the LF has an increased stability margin compared to the CTSDM, due to the conservative stability guarantees (cf. (4)). We conclude that a digital calibration is needed for the CBADC reconstruction filter, which is possible and practical, as will be shown in another paper.

V. Clock Jitter

Clock jitter is known to be one of the major performance limiting factors in CTSDM [7]. For a clock period T, the k'th rising edge will ideally arrive at a time $t_{0k} = kT$. However, in the presence of clock jitter, the clock rises at $t_{jk} = kT + \tau_k$, where the absolute clock jitter τ_k is a random variable.

For modulators with square wave feedback DAC, variations in the width of the feedback pulse is known to be the dominant source of jitter error [8], as the corresponding error signal is not shaped by the loop-filter. The performance of the modulator is therefore nearly independent of the statistical distribution of τ_k, as it is the variation in the pulse width, not in the absolute position, that limits the performance [9]. When analyzing the jitter induced error with NRZ and return-to-zero (RZ) feedback DACs, reasonably accurate results may be obtained by assuming τ_k are i.i.d. zero mean, Gaussian random variables with standard deviation σ_j.

The power spectral density (PSD) of the jitter induced error under the stated assumptions is analyzed in a number of publications, e.g. [10], [11]. In summary, the PSD of the jitter error may be expressed as

$$P_j(f) \propto \Delta \left(\frac{\sigma_j}{T}\right)^2 T, \tag{5}$$

where Δ denotes the quantizer step-width.

For the LF ADC, we would similarly expect the pulse width variations in the control signal $s_1(t)$ to be the dominant source

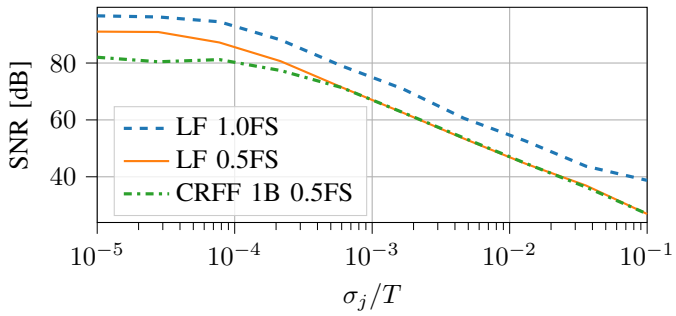

Fig. 4: Simulated SNR vs. normalized RMS jitter (σ_j/T) for a 3rd order LF and CRFF CTSDM with one bit quantizer (CRFF 1B).

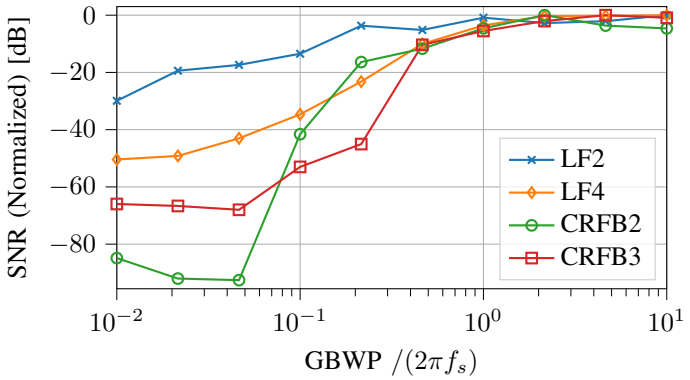

Fig. 5: Simulated normalized SNR vs. normalized amplifier GBWP, for a 2nd and 4th order LF (LF2, LF4) and a 2nd and 3rd order CRFB CTSDM (CRFB2, CRFB3).

of jitter error, as the equivalent error signal adds in parallel with the input. It is therefore reasonable to assume that the PSD of the jitter error in the LF ADC follows the same proportionality relations as described by (5).

For the clock jitter simulations, we consider it most relevant to compare architectures with the same quantizer step-width, as these would be expected to suffer similarly from jitter noise, cf. (5). Fig. 4 compares simulated SNR versus normalized RMS jitter (σ_j/T) for the 3rd order LF and the CRFF CTSDM with one bit quantizer (CRFF 1B) from Fig. 2. The figure shows that both the LF and the CTSDMs follow a -20dB/decade relationship to σ_j, as expected from (5). When simulated with the same input amplitude, the LF and CTSDM has essentially the same SNR when limited by jitter noise. However, the LF is designed for an FS amplitude which gives an SNR advantage of 6dB.

VI. Finite Amplifier Gain-Bandwidth Product

In order to draw any conclusions on the expected power consumption of a LF ADC relative to comparable CTSDMs, the power consumption of the amplifiers used to implement the active-RC integrators of the loop filter must be taken into account. In particular the first amplifier, whose errors are not suppressed by the loop filter, is often the most power-hungry component of the whole modulator [12]. In the CTSDM literature, the power consumption is often assumed to be proportional to the required GBWP [13], defined as

$$\text{GBWP} \triangleq 2\pi A_0 f_u, \tag{6}$$

where A_0 is the DC-gain of the amplifier and f_u denotes the open-loop unity gain frequency. To obtain some insight in the expected power consumption of the LF ADC we therefore compare the sensitivity to the amplifier's GBWP.

Simulated (normalized) SNR versus amplifier GBWP is shown in Fig. 5 for a 2nd and 4th order LF (LF2, LF4) and a 2nd and 3rd order CRFB CTSDM (CRFB2, CRFB3). In the simulations, the GBWP of all amplifiers are varied by the same amount. The OSR values are the same as used in the simulations of Fig. 2. However, due to stability issues, $||\text{NTF}||_\infty$ was reduced to 1.3 for the CTSDMs, compared to the optimized value used for the simulations in Fig. 2. Despite the reduced NTF gain, the CTSDMs still suffer from stability issues for smaller GBWPs, which is seen in Fig. 5 for normalized SNR values below -40dB. For the LF simulations, the filter coefficients of (2) has been modified to account for the internal amplifier pole, such that the filter error described in Section IV is avoided.

The main observation from Fig. 5 is that both the LFs and CTSDMs approach their nominal SNR for GBWP $\approx 2\pi fs$. This coindices with previous studies on CTSDMs concluding that an amplifier unity gain frequency of $f_u \approx f_s$ is needed, unless the finite GBWP is compensated by modifying the loop filter coefficients [13]. Similar compensation techniques could be derived for the LF as well; however, simulations with GBWP compensation is beyond the scope of this paper.

The simulated sensitivity to the amplifiers' GBWP indicate that the LF and CI impose similar requirements on the amplifiers as a CTSDM with the same f_s and filter order N. We find it reasonable to conclude that the analog system of a LF ADC is expected to have a similar power consumption as the loop filter of a comparable CTSDM.

VII. Conclusions

Through behavioural circuit simulations, the CI and LF CBADC have been compared to relevant CTSDMs in terms of nominal performance and sensitivity to clock jitter, component variations and finite GBWP in the amplifiers.

It was shown that the LF and CI ADC have a similar nominal performance as a CTSDM of the same order and with the same number of quantization levels, but with a larger stability margin and the benefit of only using single-bit quantizers.

Without calibration, the mismatch between the reconstruction filter and analog system makes any CBADC sensitive to component variations. However, if corrected for, the LF

displays a larger tolerance to time constant variations than a correspondingly parameterized CTSDM.

The CI and LF's sensitivity to clock jitter and finite GBWP is comparable to that of a CTSDM. Simulations with finite GBWP show that the amplifier's unity gain frequency should be on the order of $f_u \approx f_s$ to avoid significant performance degradation.

The presented comparison results shows that the LF ADC could be an interesting alternative to conventional CTSDM. It has the benefit of a simple, modular structure with an analytical stability guarantee and single-bit quantizers.

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